

Correlation table (I) between a variety of combination configurations and advantageous effect number

Combination advantageous effect number	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭
A) File or folder separation between SD and HD	○		○		○		○		○		△	△		△
B) 4 bit expression of sub-picture information and compression rule		○		○		○		○		○	△	△		△
C) Plural types of recording formats can be set for read only					○	○	△	△	△	△	○			
D) ECC block structure using multiplication code					○	○	○	○	○	○	○			
E) Sector is divided into a plurality of small ECC blocks							○	○			○			
F) PO group data which are different from each other on sector by sector basis are inserted									○	○				
G) Physical segment division structure in ECC block			○	○	○	○	△	△	△	△	○	△	○	△
H) Guard region allocation structure between ECC blocks			△	△	○	○					○			
I) Partial duplication is recorded in guard area											○			
J) Number of code changes ≥ 2 when combination of SYNC codes is shifted	○	○					○	○	○	○				
K) Occupancy rate of non-modulation region is set to be higher than modulation region													○	
L) L/G recording + Wobble modulation	○	○	○	○										○
M) Uncertain bits are allocated to be distributed to group region												○		○
N) Uncertain bits are allocated to be distributed to Land and Groove												○		
O) Wobble phase modulation of ± 90 degrees												△	○	
P) Gray code or specific track code is employed	○	○												
Q) SYNC code or SYNC data structure in guard region	△	△			○	○	○	○	○	○				
R) Tp · Pp is roughened in System Lead-in area							○	○	○	○				
S) Signal reproduction processing using PRML technique is carried out	○	○					○	○						
T) Modulation rule of $d = 1$ is employed	△	△					○	○	○	○				
U) Configuration by data segment having one or more recording clusters					○	○					○			

FIG.1

Correlation table (II) between a variety of combination configurations and advantageous effect number

Combination advantageous effect number	(15)	(16)	(17)	(18)	(19)	(20)	(21)	(22)	(23)	(24)	(25)	(26)	(27)	(28)
A) File or folder separation between SD and HD	△	△				○		△	○		○	△		
B) 4 bit expression of sub-picture information and compression rule	△	△					○	△	○		○	△		
C) Plural types of recording formats can be set for read only		○										△		
D) ECC block structure using multiplication code	○	○		○				○				△		
E) Sector is divided into a plurality of small ECC blocks	○	△		○				○				△		
F) PO group data which are different from each other on sector by sector basis are inserted	○	△		○				○				△		
G) Physical segment division structure in ECC block	○											○	○	
H) Guard region allocation structure between ECC blocks		○			○								○	
I) Partial duplication is recorded in guard area		△											○	
J) Number of code changes ≥ 2 when combination of SYNC codes is shifted	○	○			○							○		
K) Occupancy rate of non-modulation region is set to be higher than modulation region											○	○	○	
L) L/G recording + Wobble modulation									○	○	○		△	
M) Uncertain bits are allocated to be distributed to group region										○	○			
N) Uncertain bits are allocated to be distributed to Land and Groove										○				
O) Wobble phase modulation of ± 90 degrees										○				
P) Gray code or specific track code is employed											○			
Q) SYNC code or SYNC data structure in guard region		○			○							○		
R) Tp · Pp is roughened in System Lead-in area			○	○	○									
S) Signal reproduction processing using PRML technique is carried out			○			○	○	○	○		○			
T) Modulation rule of $d = 1$ is employed			○			○	○				○			
U) Configuration by data segment having one or more recording clusters		○											○	

FIG.2

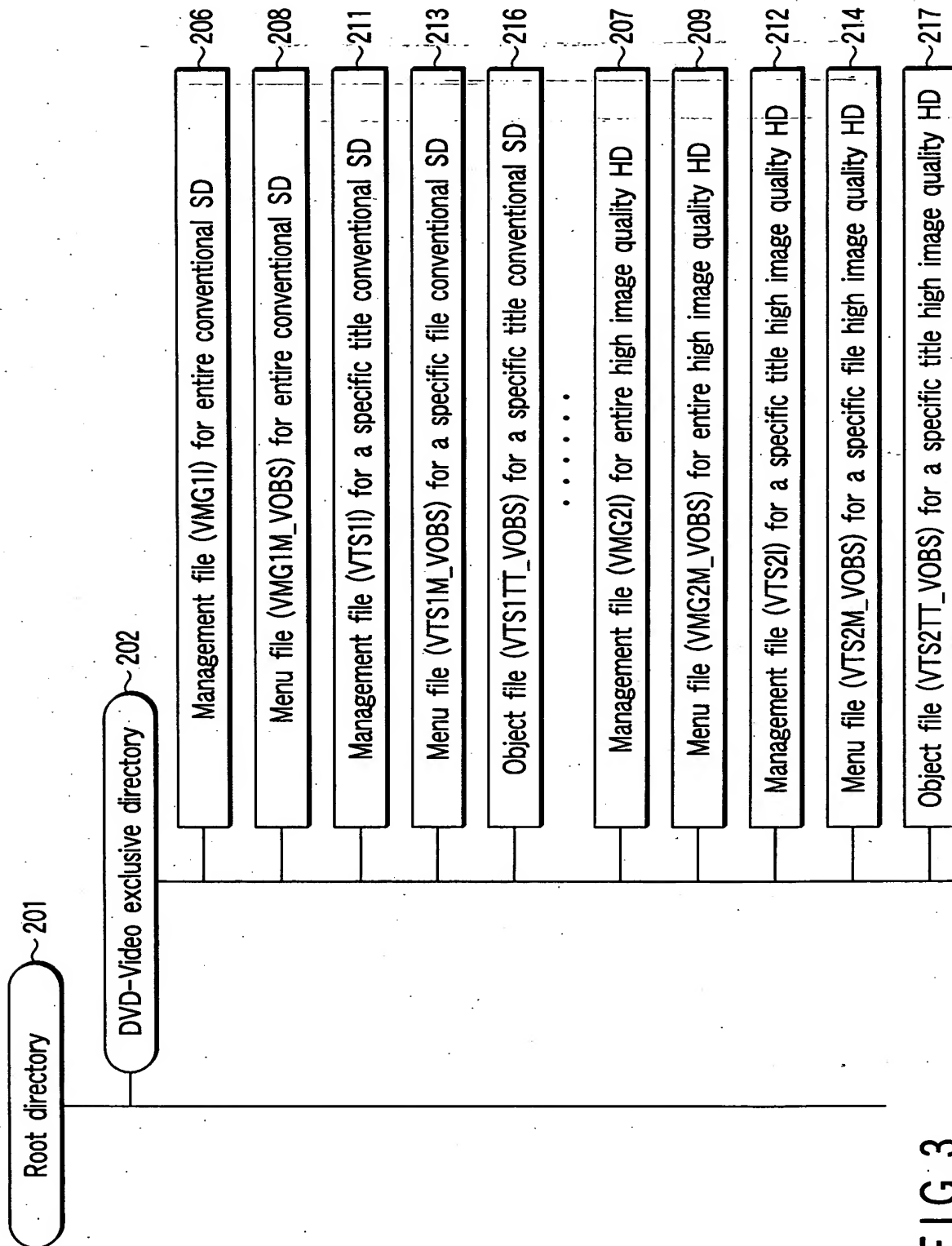


FIG. 3

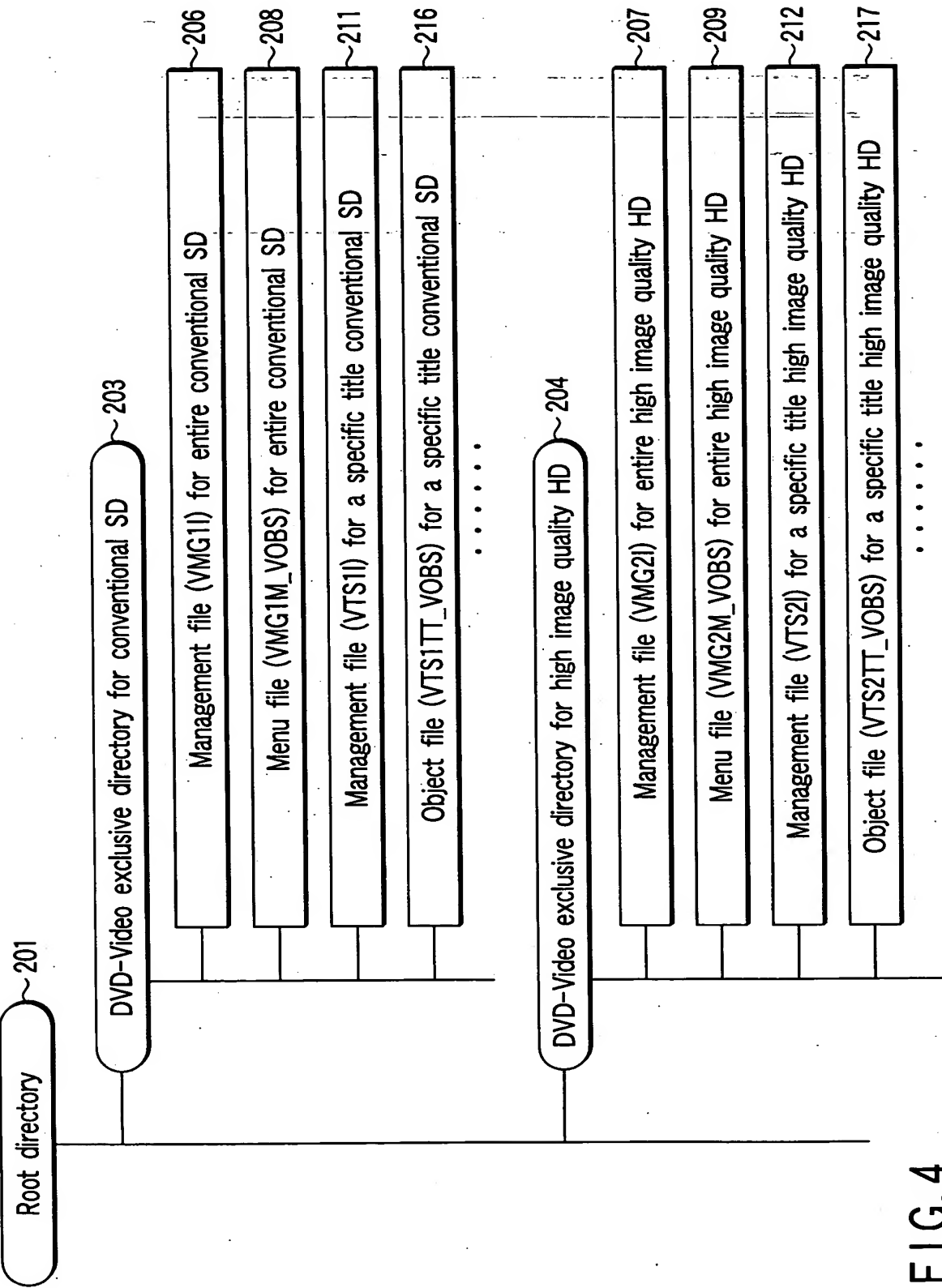


FIG. 4

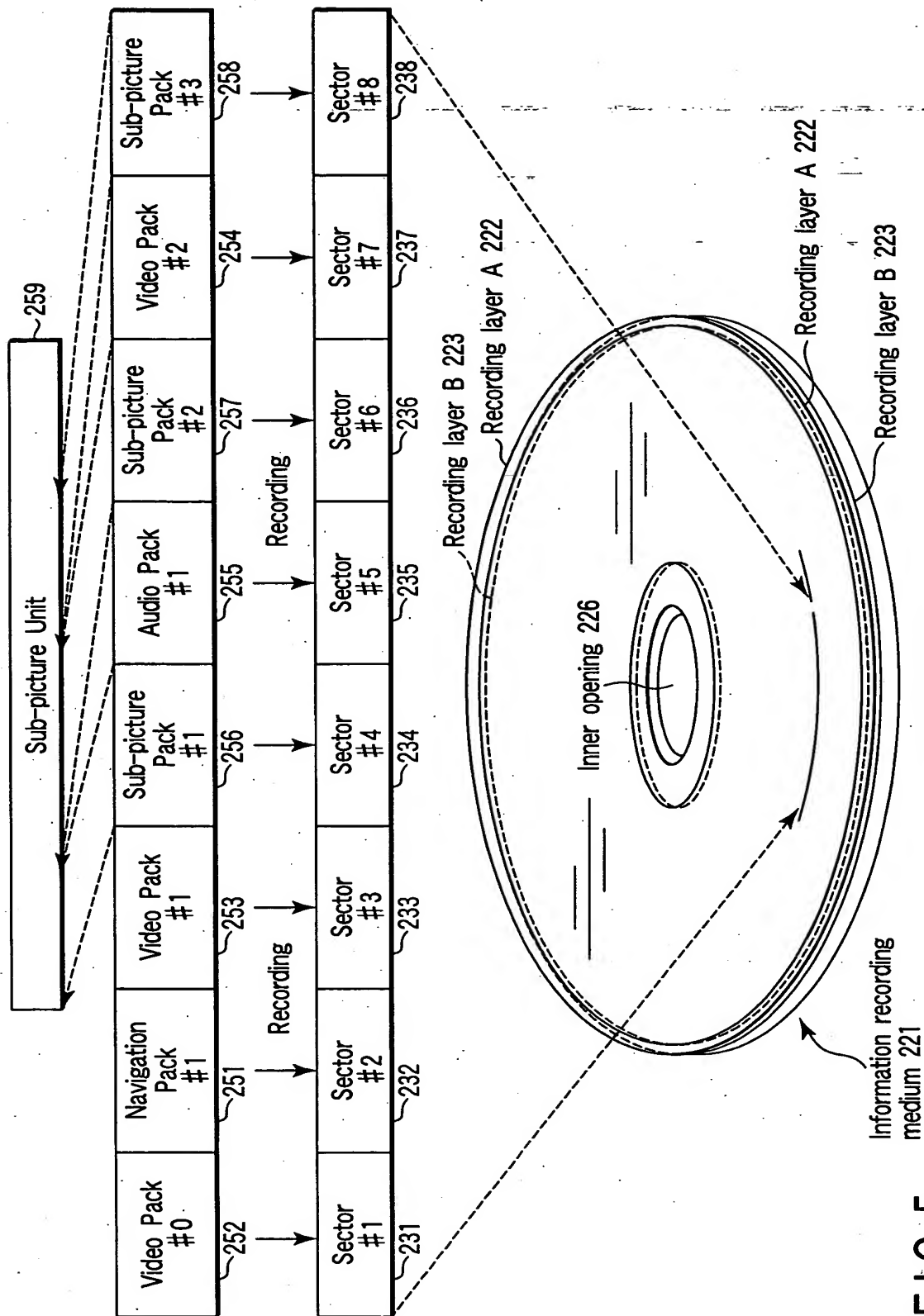


FIG. 5

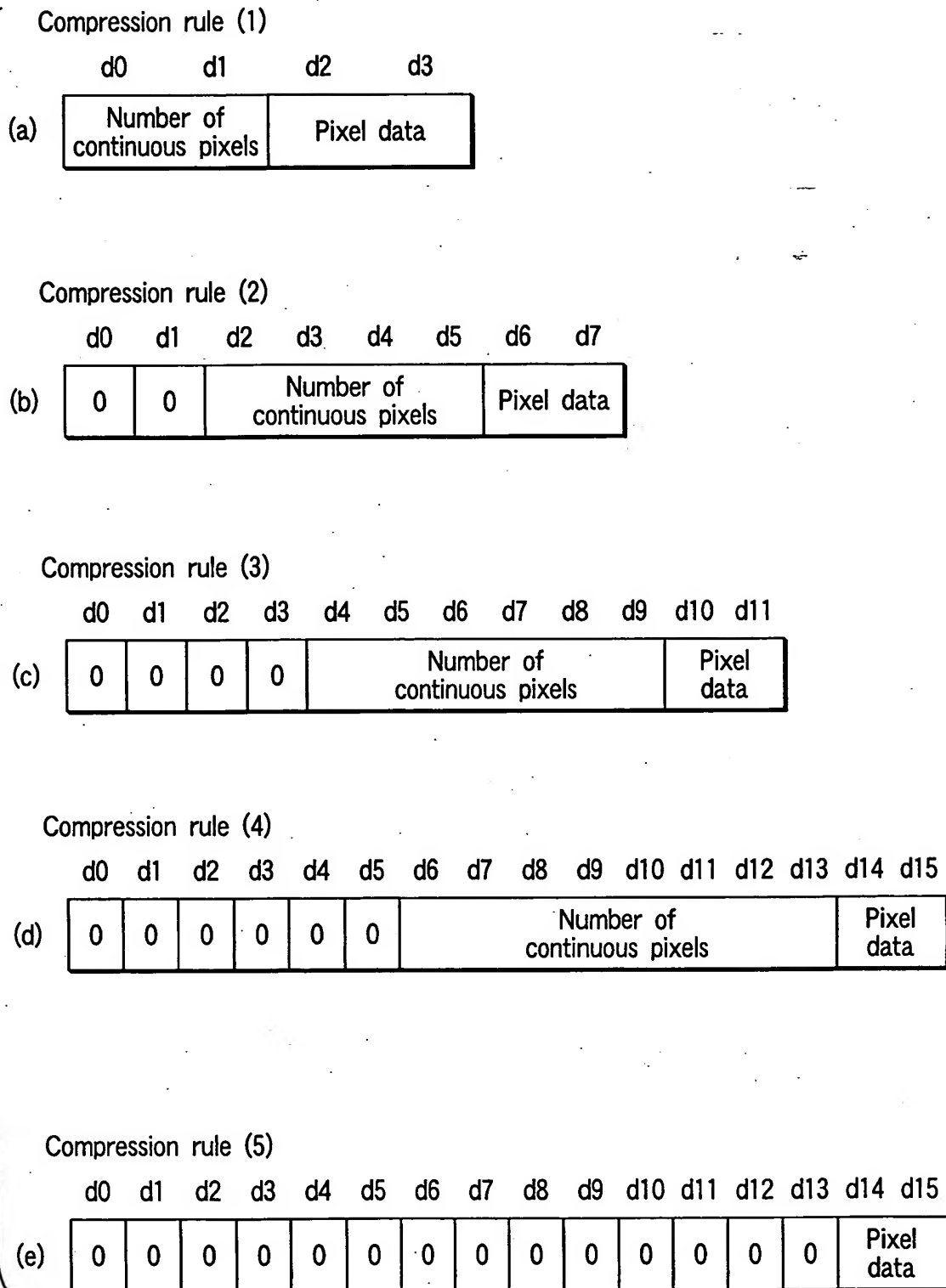


FIG. 6

Allocation of pixel data

Pixel name	Pixel data
Pixel 1	0000
Pixel 2	0001
Pixel 3	0010
Pixel 4	0011
Pixel 5	0100
Pixel 6	0101
Pixel 7	0110
Pixel 8	0111
Pixel 9	1000
Pixel 10	1001
Pixel 11	1010
Pixel 12	1011
Pixel 13	1100
Pixel 14	1101
Pixel 15	1110
Pixel 16	1111

FIG. 7

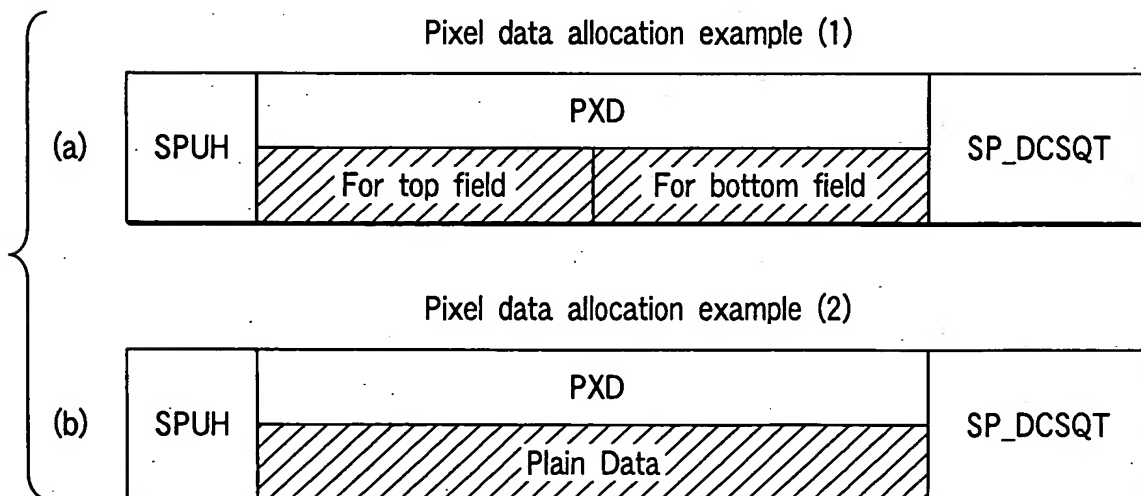


FIG. 8

Sub-picture unit (SPU) and sub-picture pack (SP_PCK)

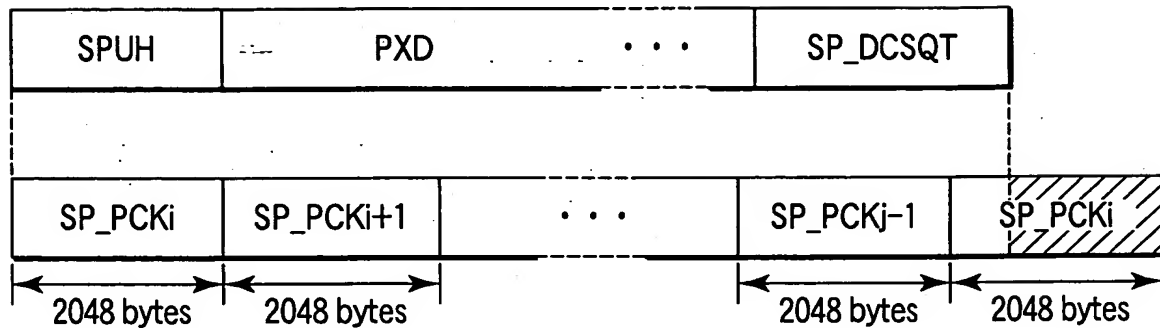


FIG. 9

Sub-picture unit header (SPUH)

Description order

	Contents	Number of bytes
(1)SPU_SZ	Size of sub-picture unit	4 bytes
(2)SP_DCSQT_SA	Start address of display control sequence table	4 bytes
(3)PXD_W	Width of pixel data	4 bytes
(4)PXD_H	Height of pixel data	4 bytes
(5)SP_CAT	Sub-picture category	1 byte
Reserved	Reserved	1 byte
	Total	18 bytes

FIG. 10

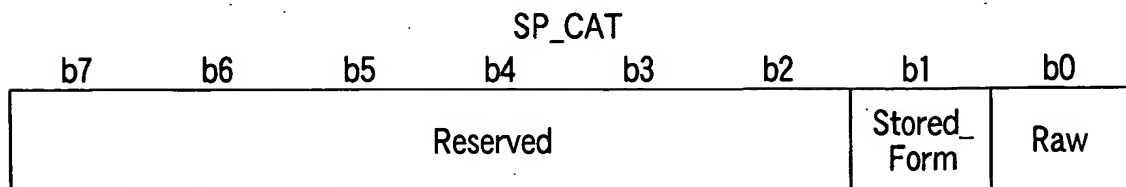


FIG. 11

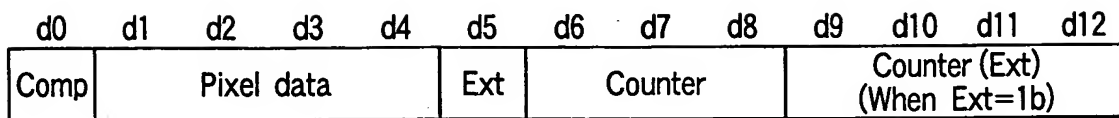


FIG. 12

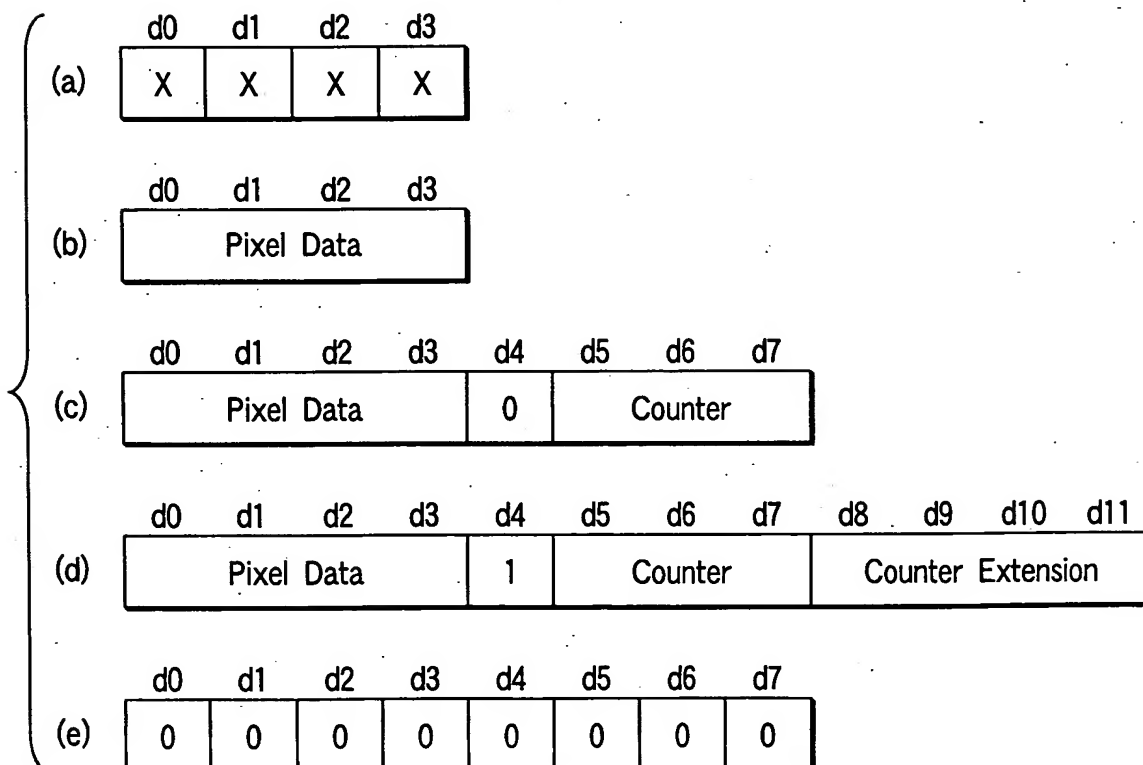


FIG. 13

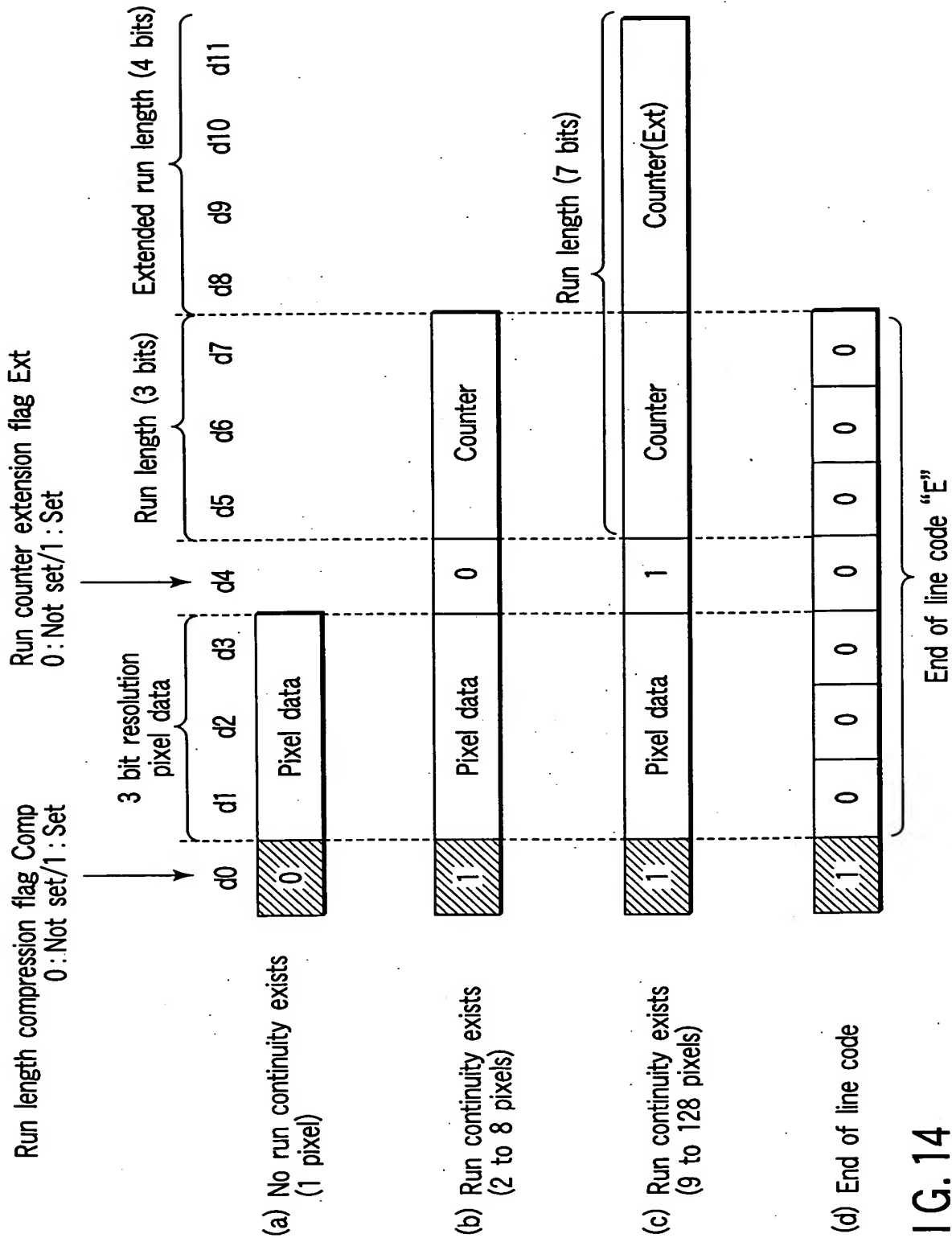


FIG. 14

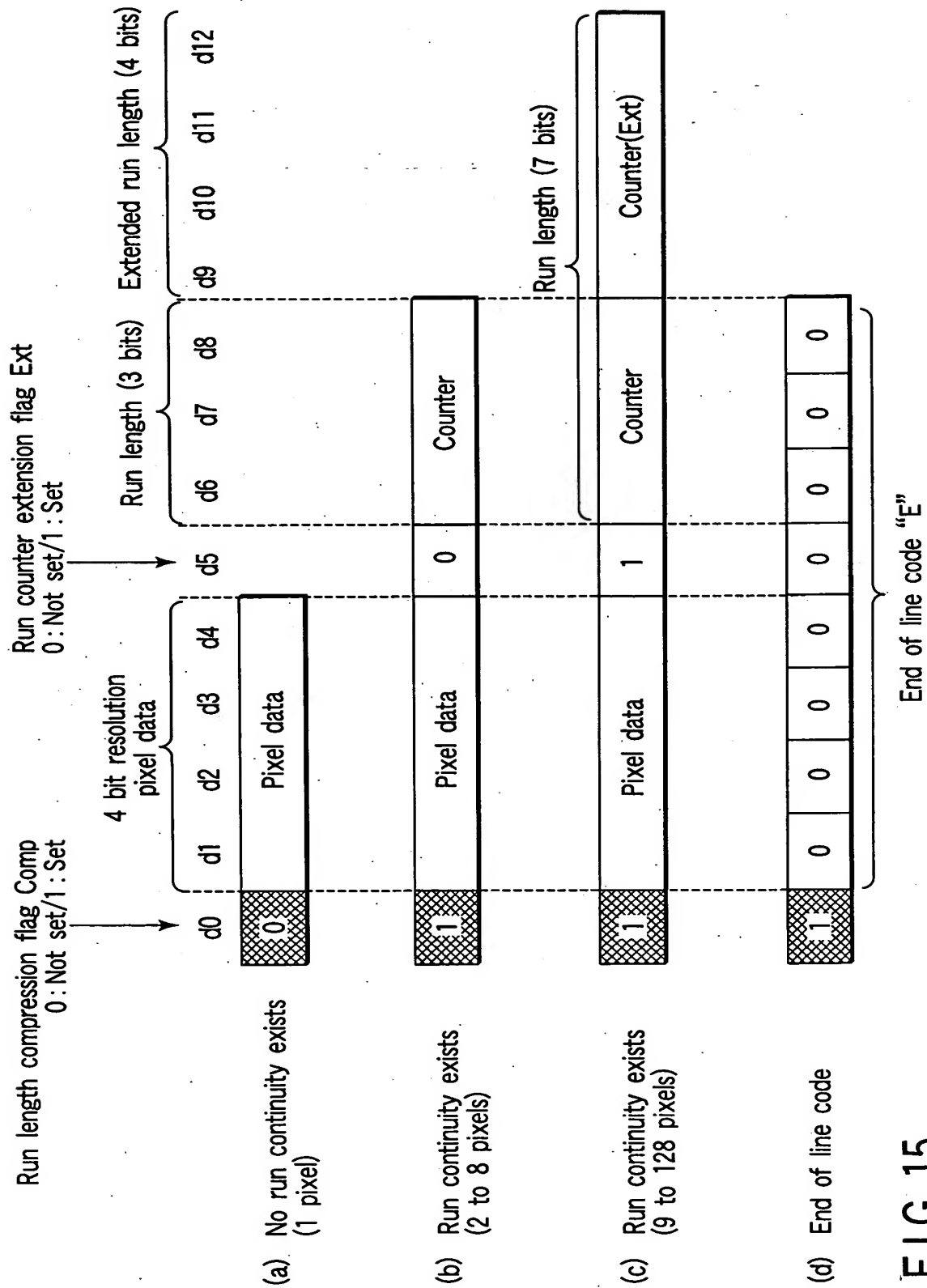
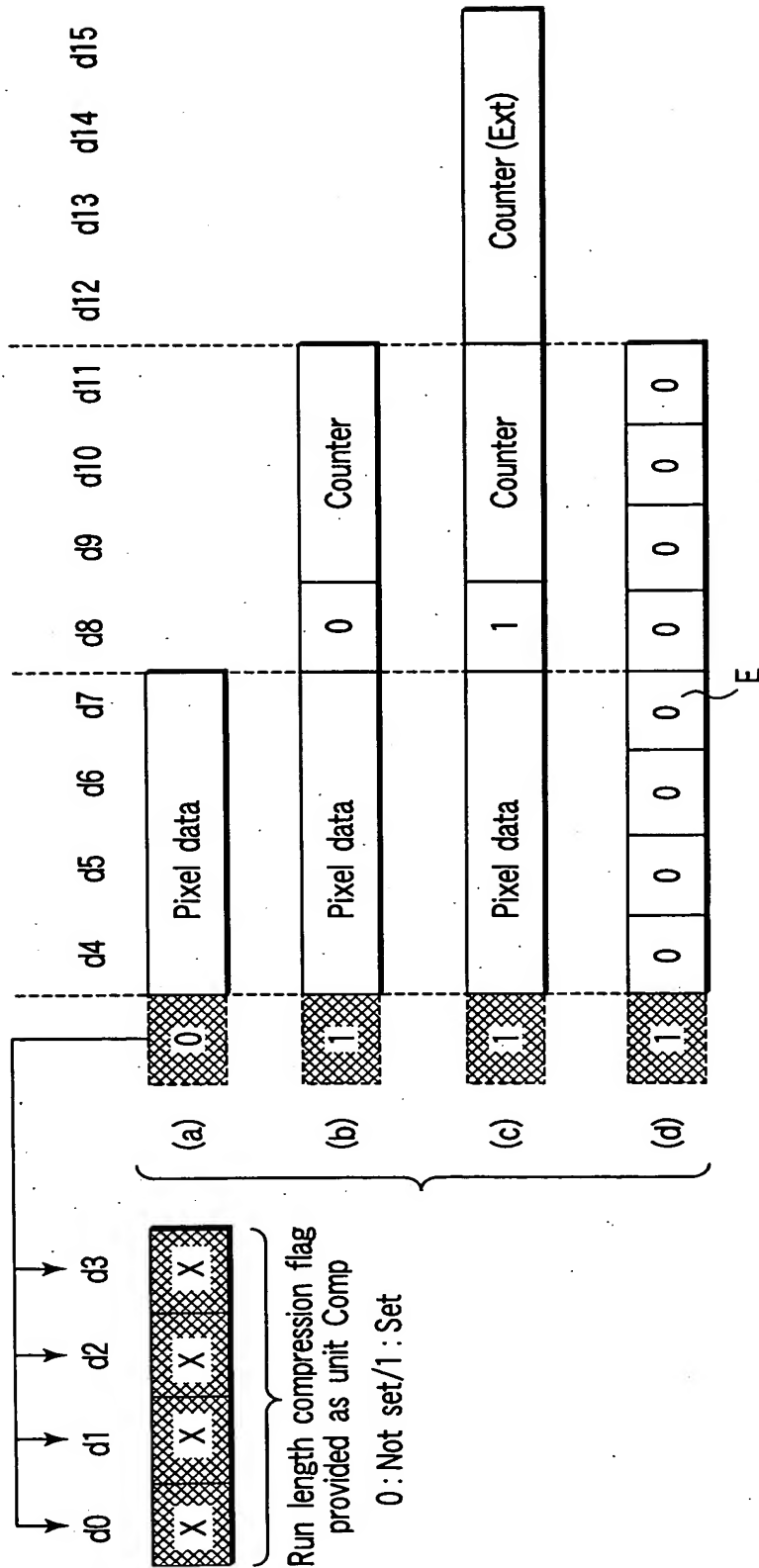


FIG. 15



※To be provided as unit in patterns of (a) to (d)

FIG. 16

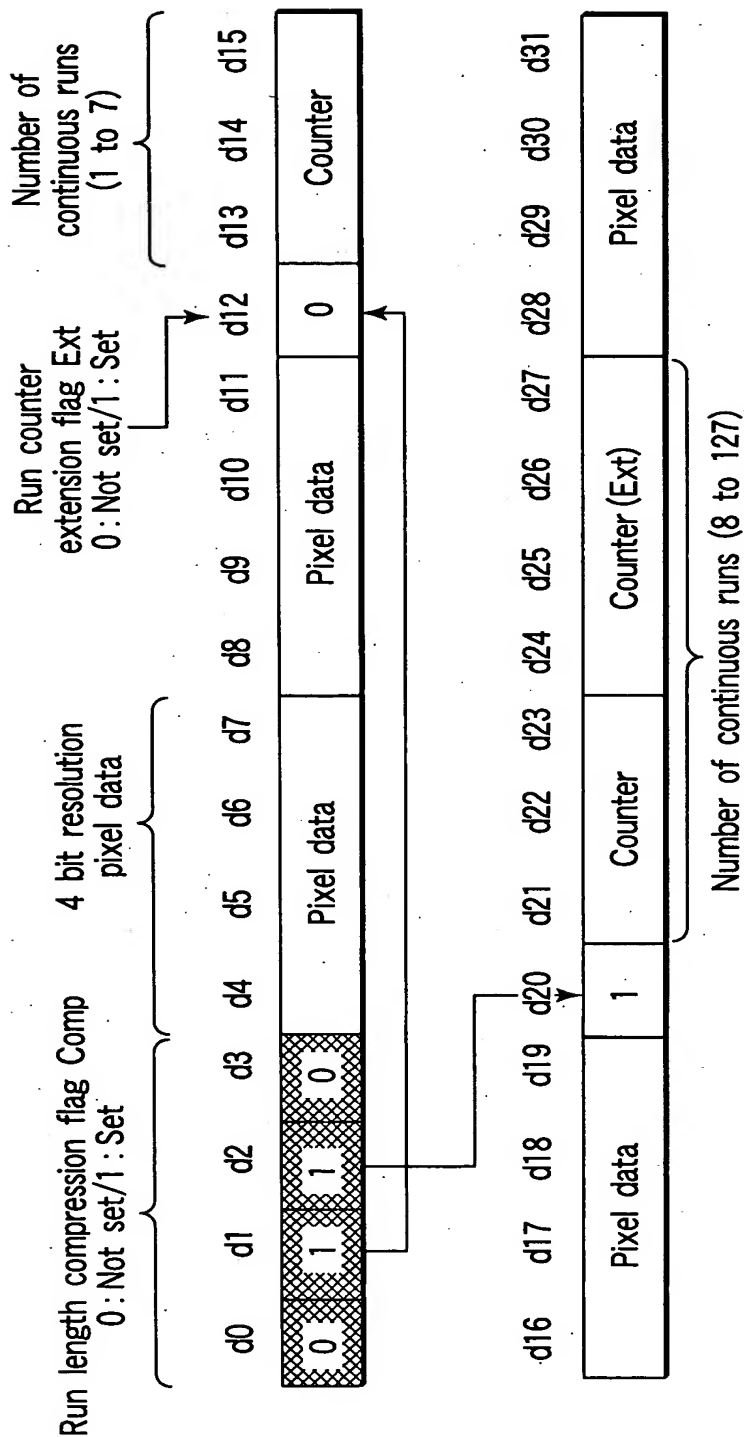
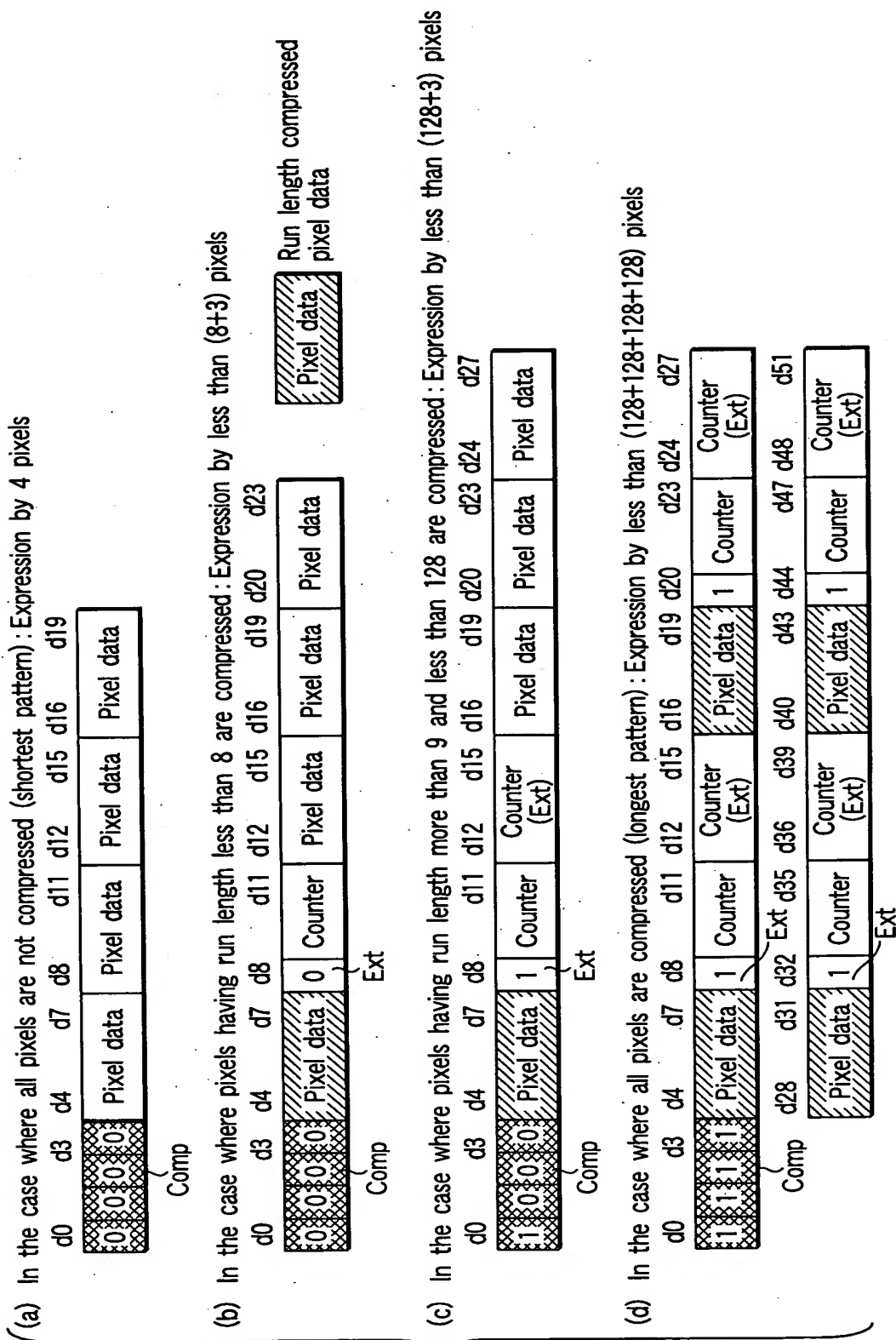


FIG. 17



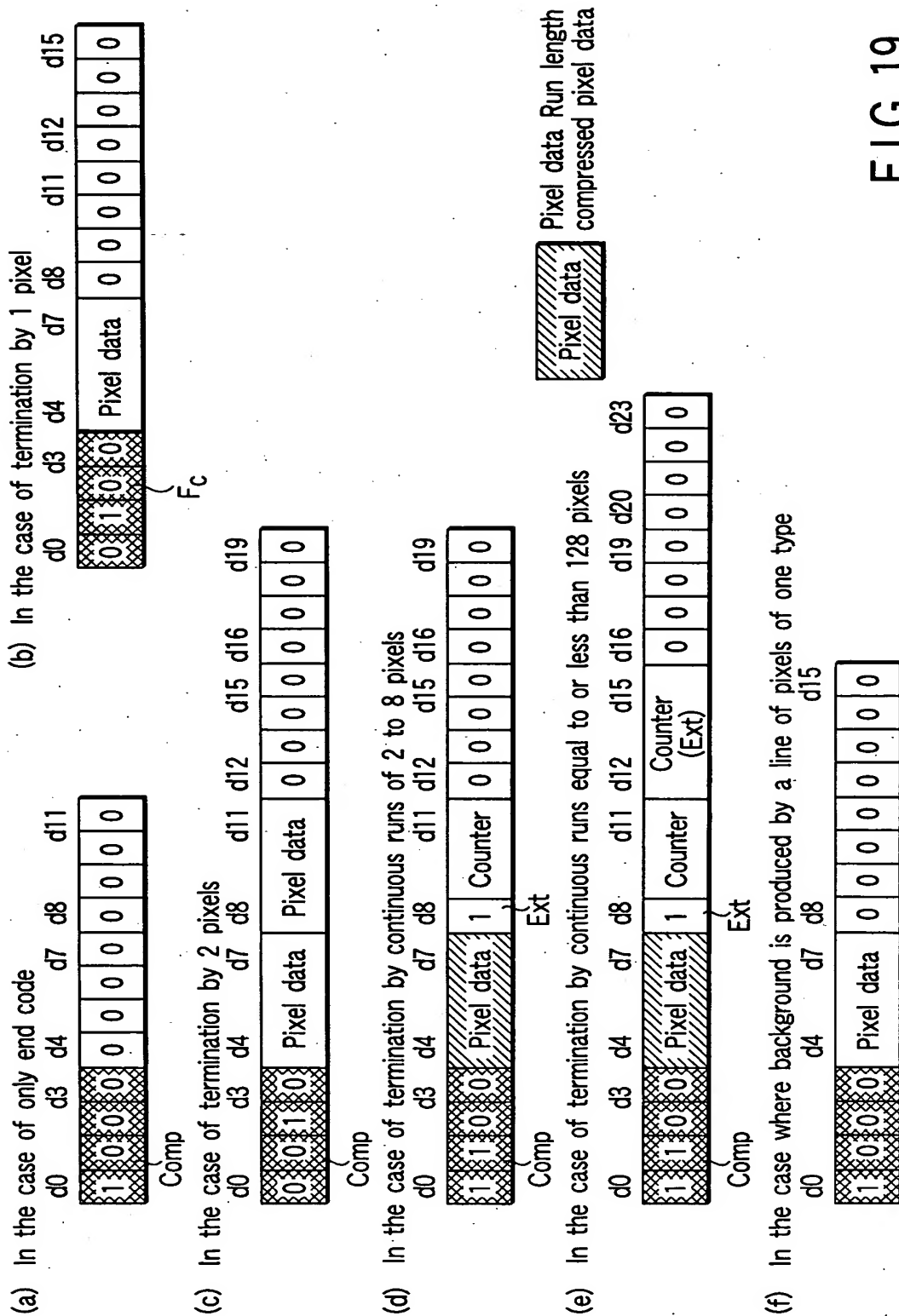


FIG. 19

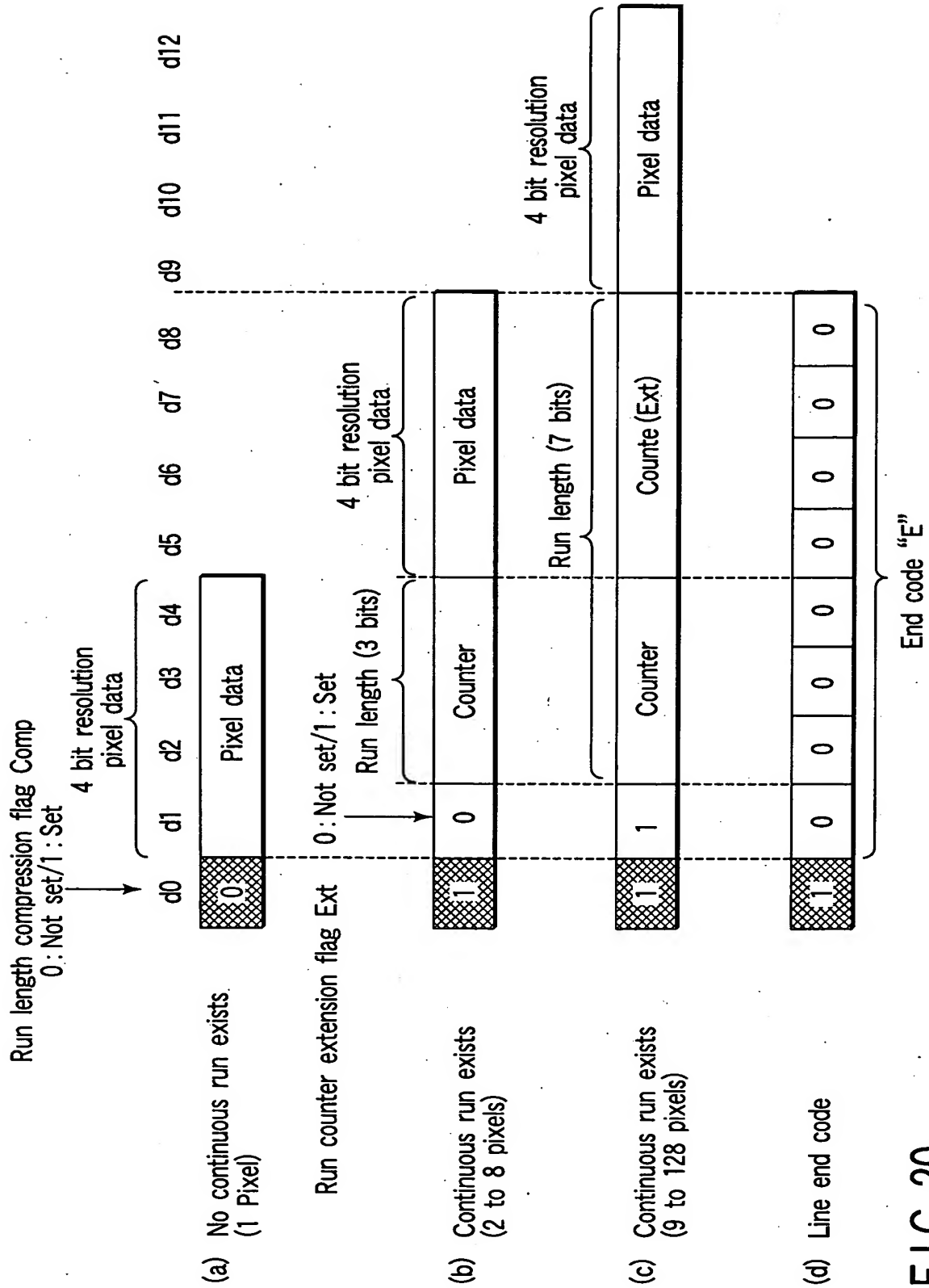


FIG. 20

(a)

Display control sequence table (SP_DCSQT) Description order

	Contents
SP_DCSQ #0	Display control sequence #0
SP_DCSQ #1	Display control sequence #1
:	
:	
SP_DCSQ #n	Display control sequence #n

(b)

Display control sequence (SP_DCSQ) Description order

	Contents	Number of bytes
(1)SP_DCSQ_STM	Start time of SP_DCSQ	2 bytes
(2)SP_NXT_DCSQ_SA	Start address of next SP_DCSQ	4 bytes
(3)SP_DCCMD #1	Display control command #1	
:	:	
SP_DCCMD #n	Display control command #n	

(c)

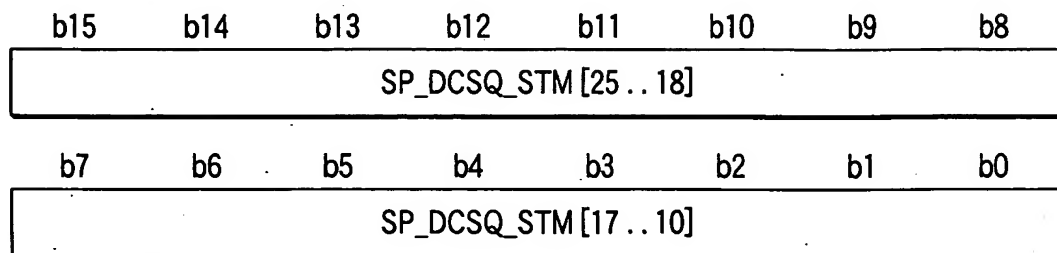


FIG. 21

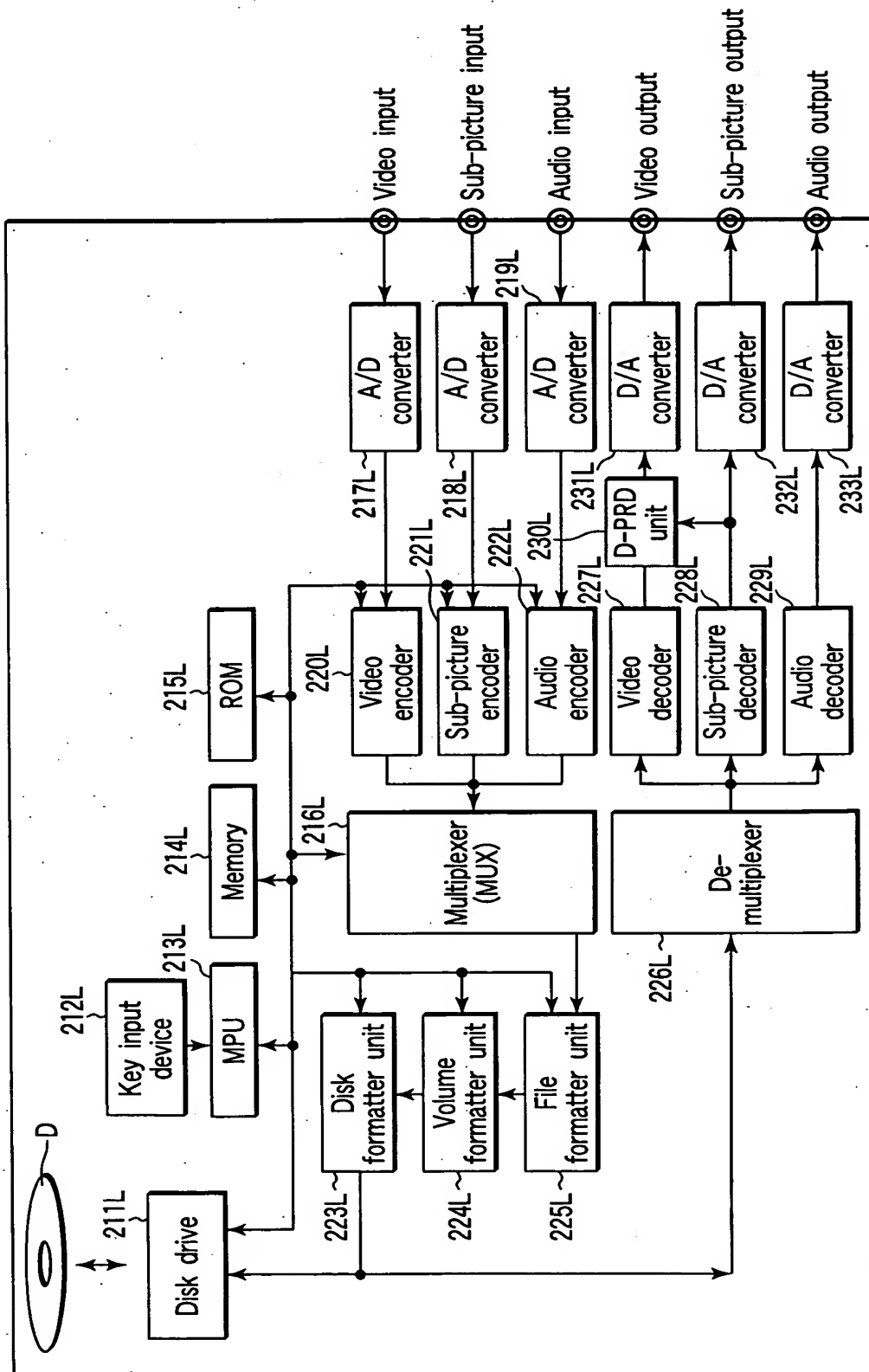


FIG. 22

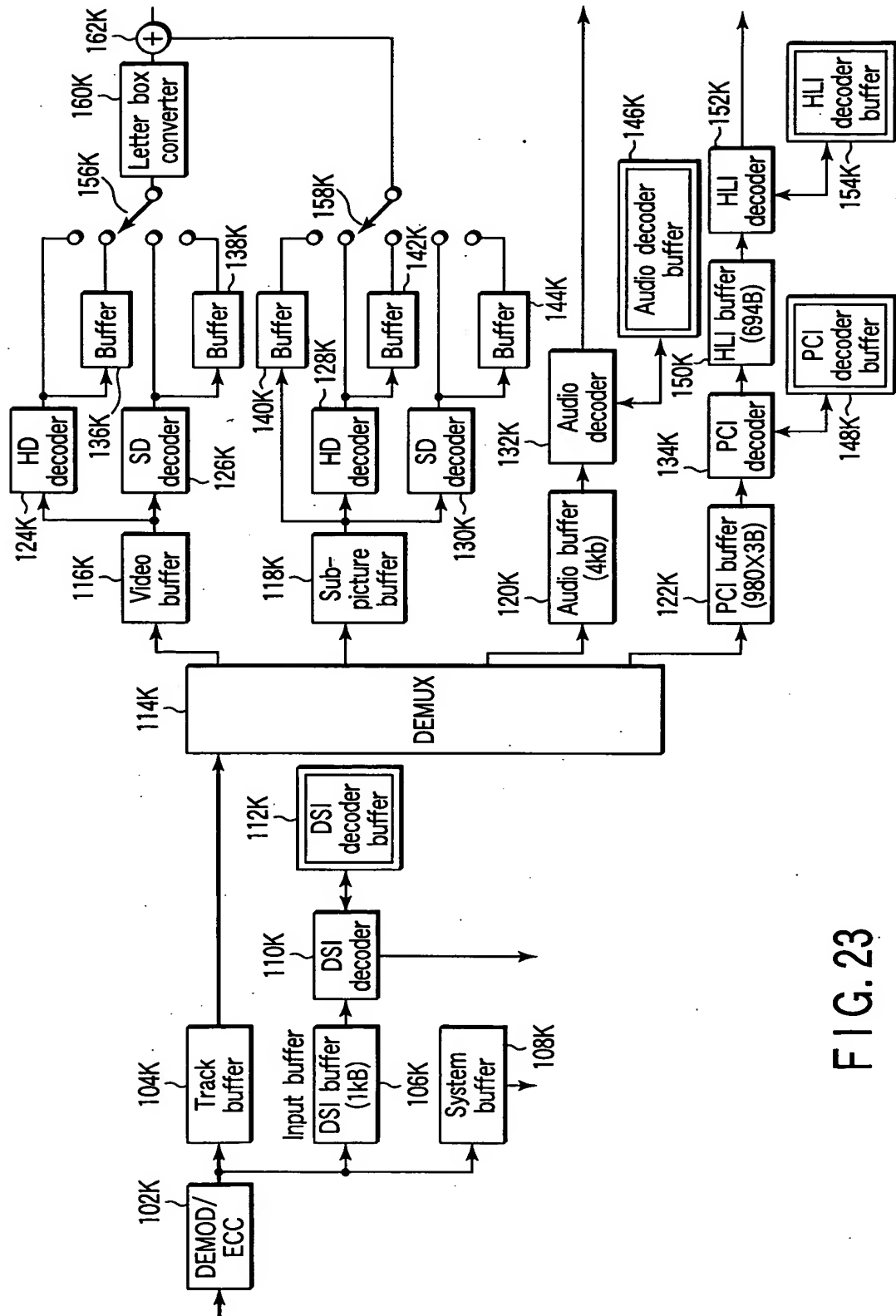


FIG. 23

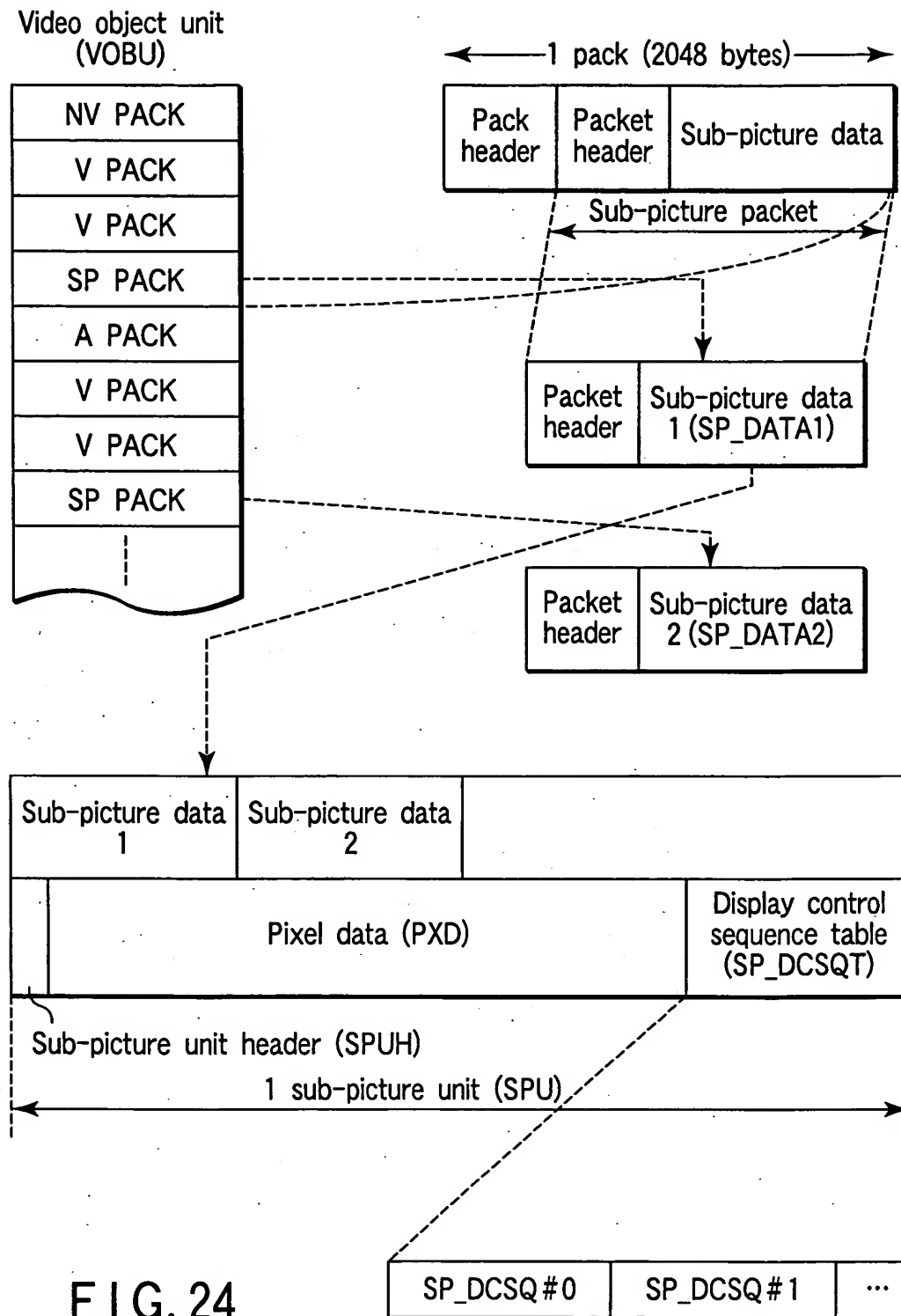


FIG. 24

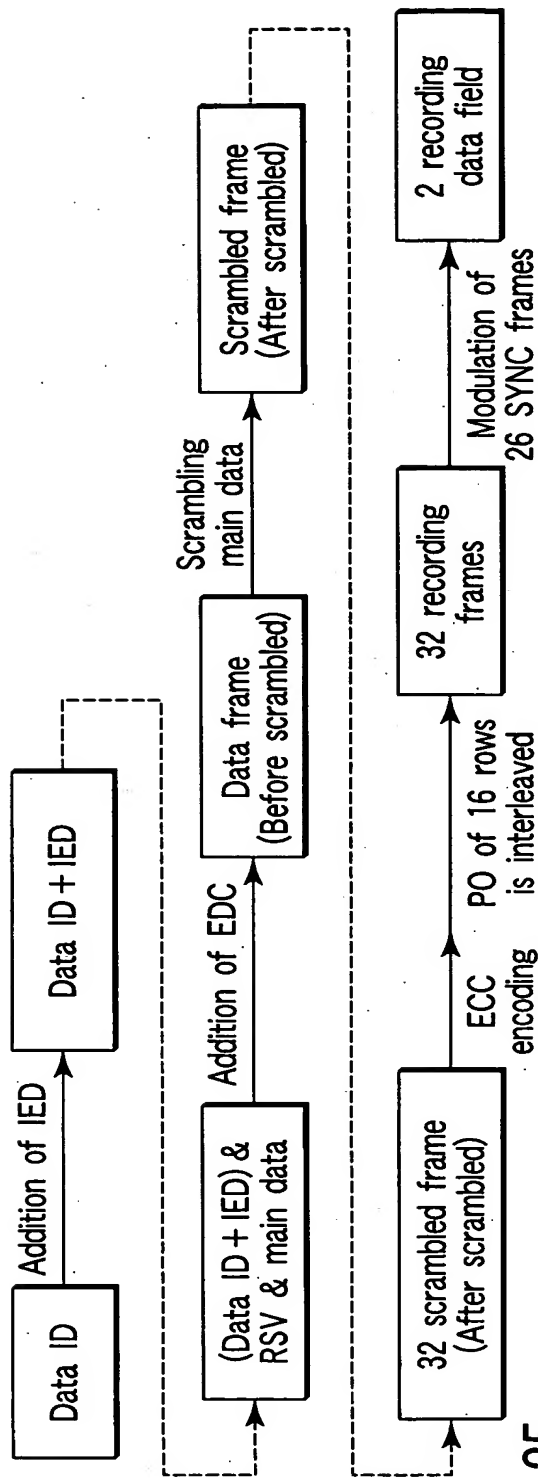


FIG. 25

Data structure in data ID

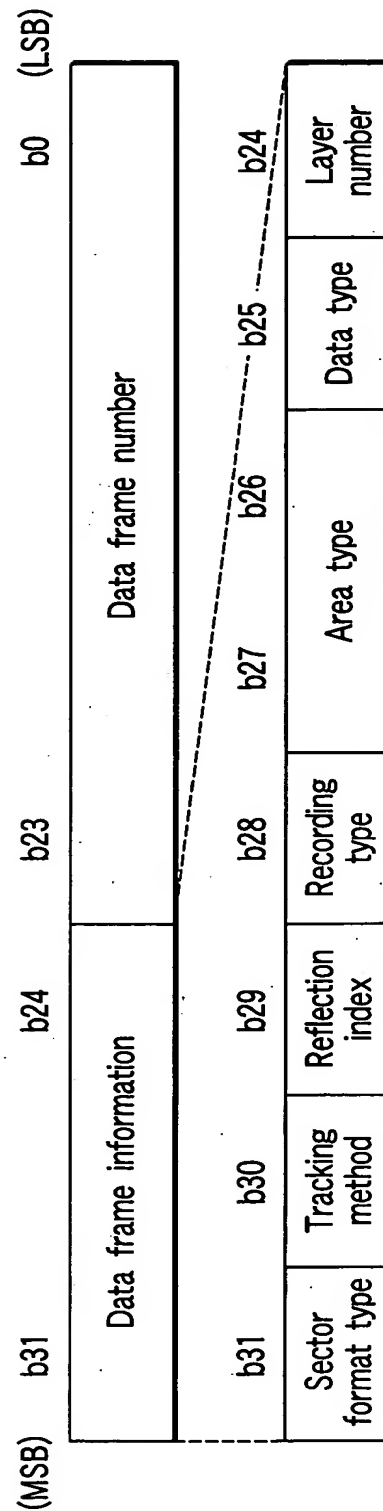


FIG. 27

Data frame structure

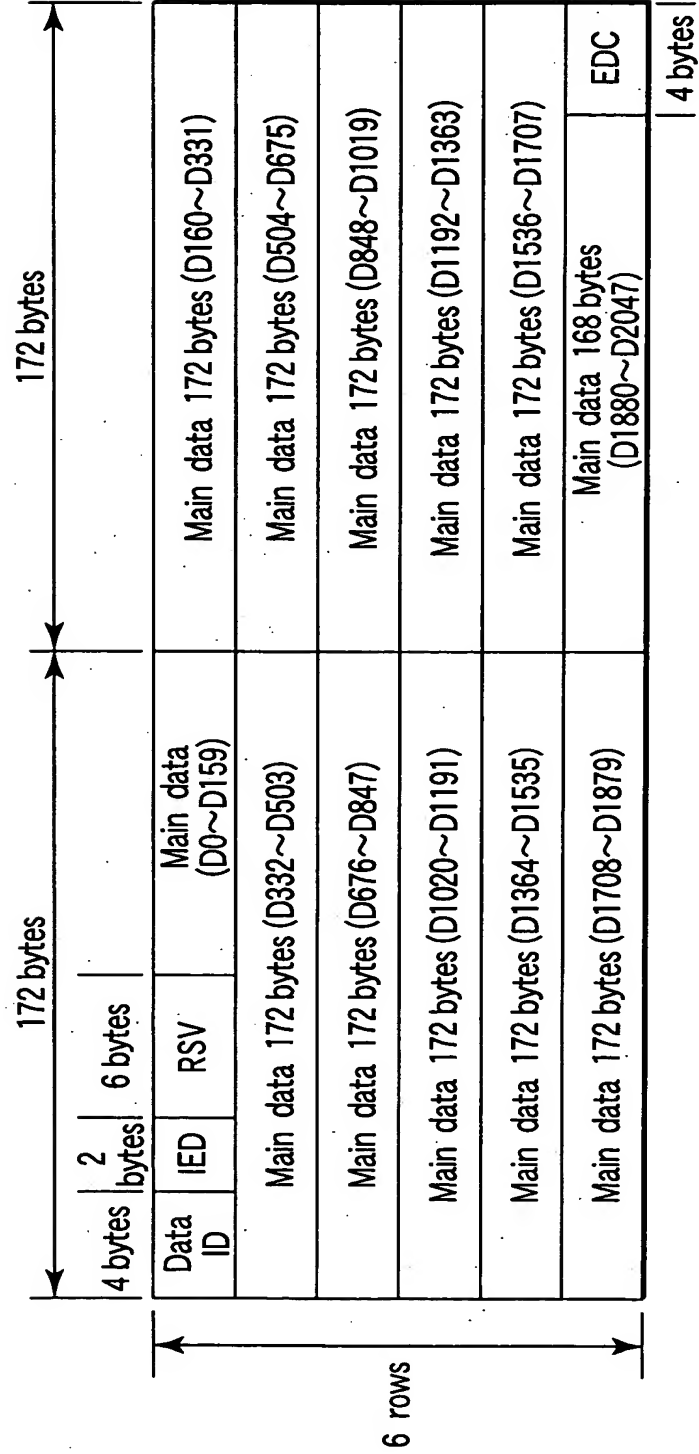


FIG. 26

Data frame number in rewritable information recording medium

Area	Contents
System lead-in area	Physical sector number
Defect management area	Physical sector number
Disk identification zone	Physical sector number
Used block of data area	LSN + 030000h
Unused block of data area	State 1 0 is set for first 3 bits of first sector, and contents are incremented for remaining sectors State 2 From 00 0000h to 00 001Fh State 3 Unrecorded

FIG. 28

Contents of record type in rewritable information recording medium

Area	Contents
System lead-in area	0b
Lead-in area, Lead-out area	0b
Data area	0b : General data 1b : Real time data

FIG. 29

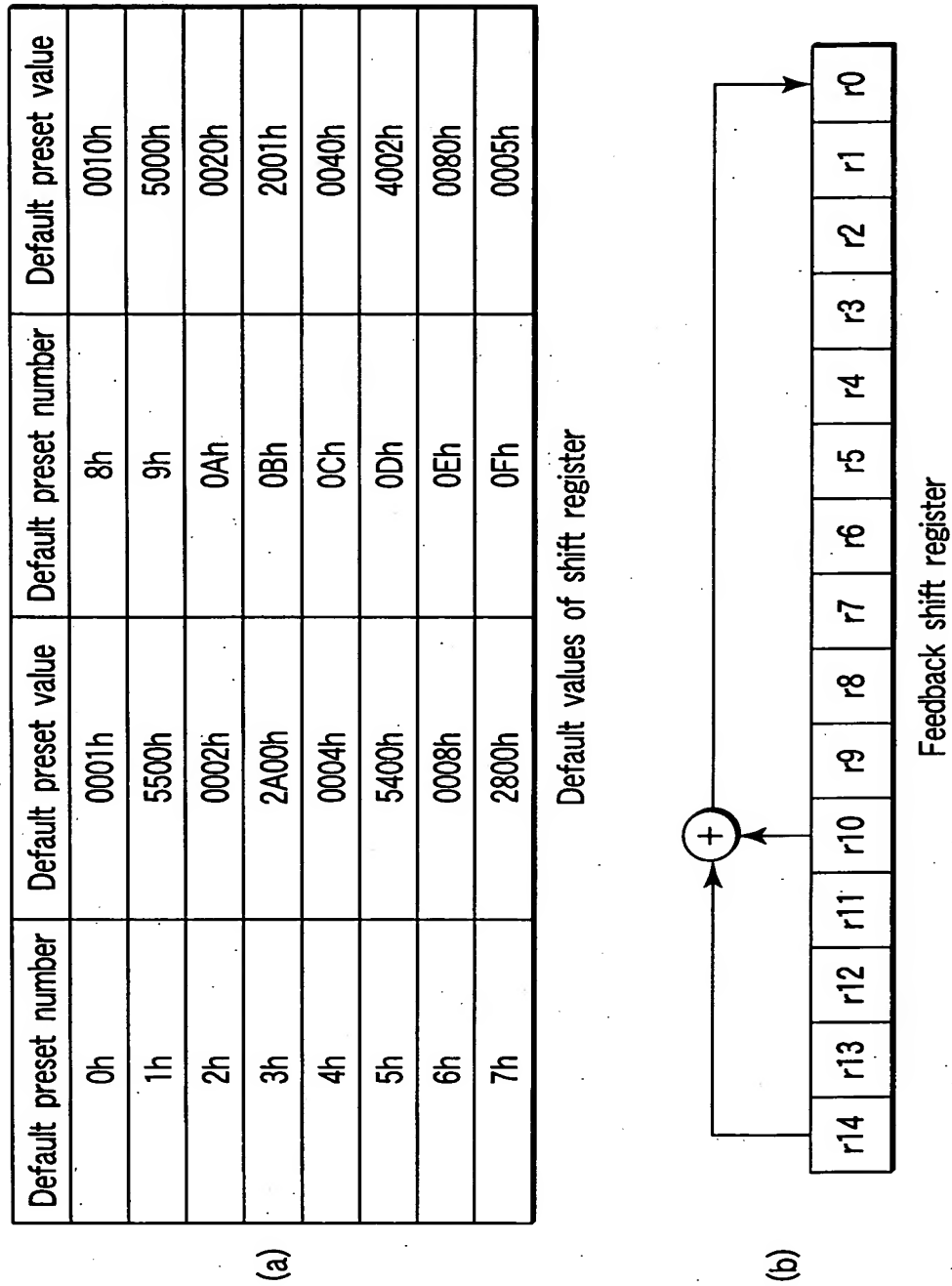


FIG. 30

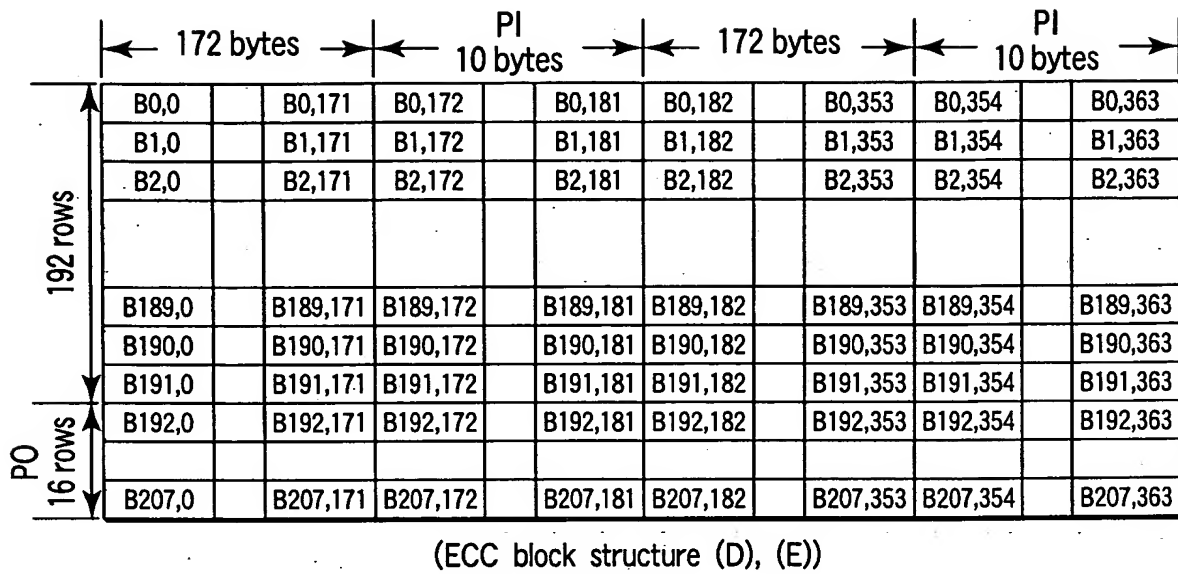


FIG. 31

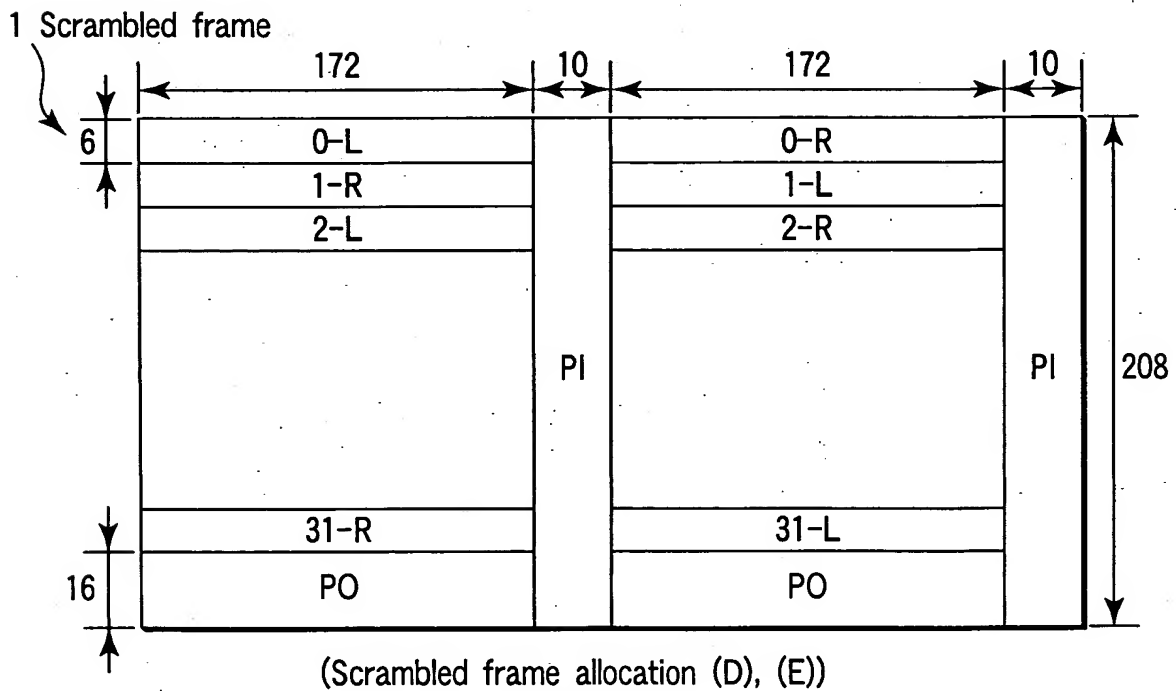


FIG. 32

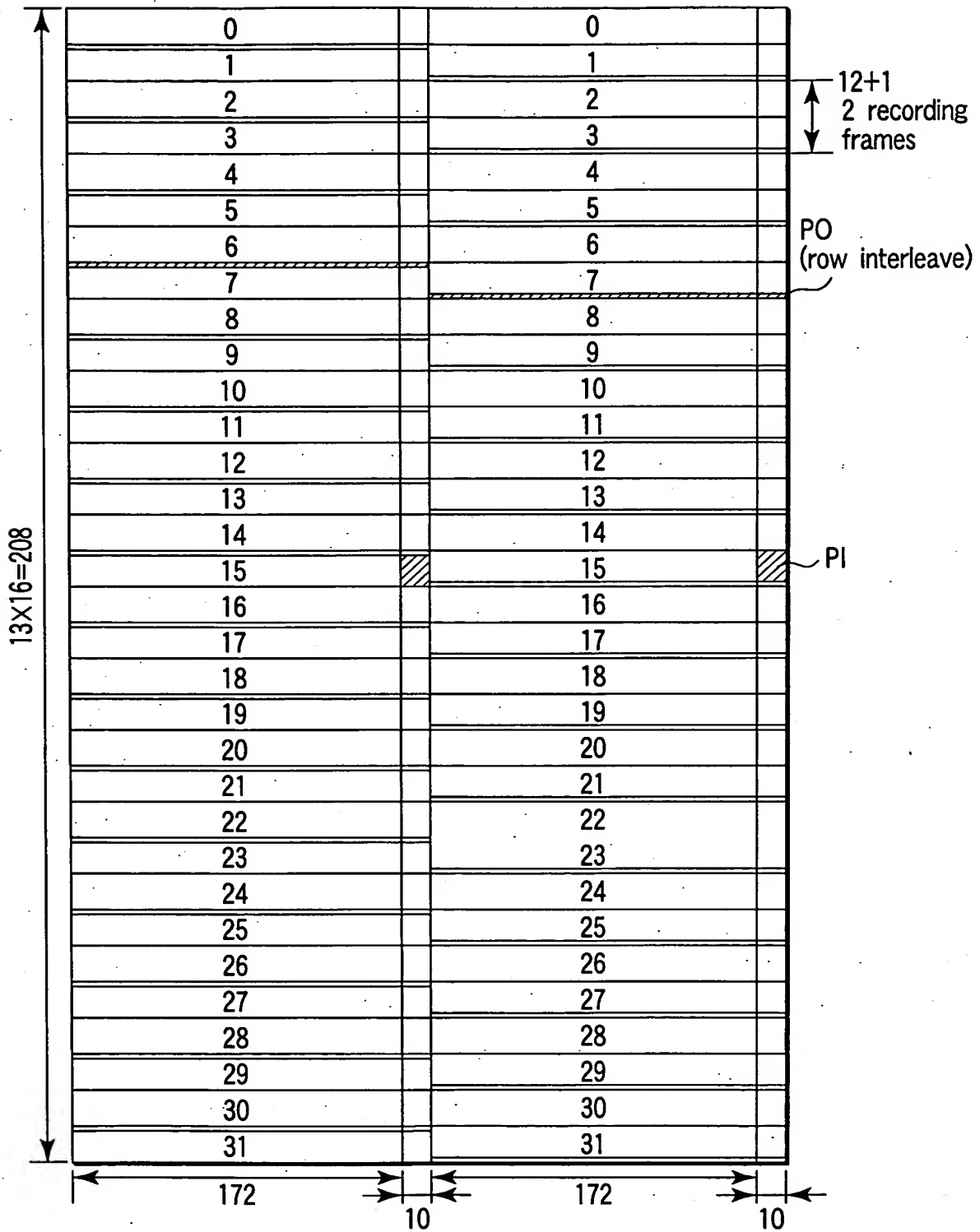


FIG. 33

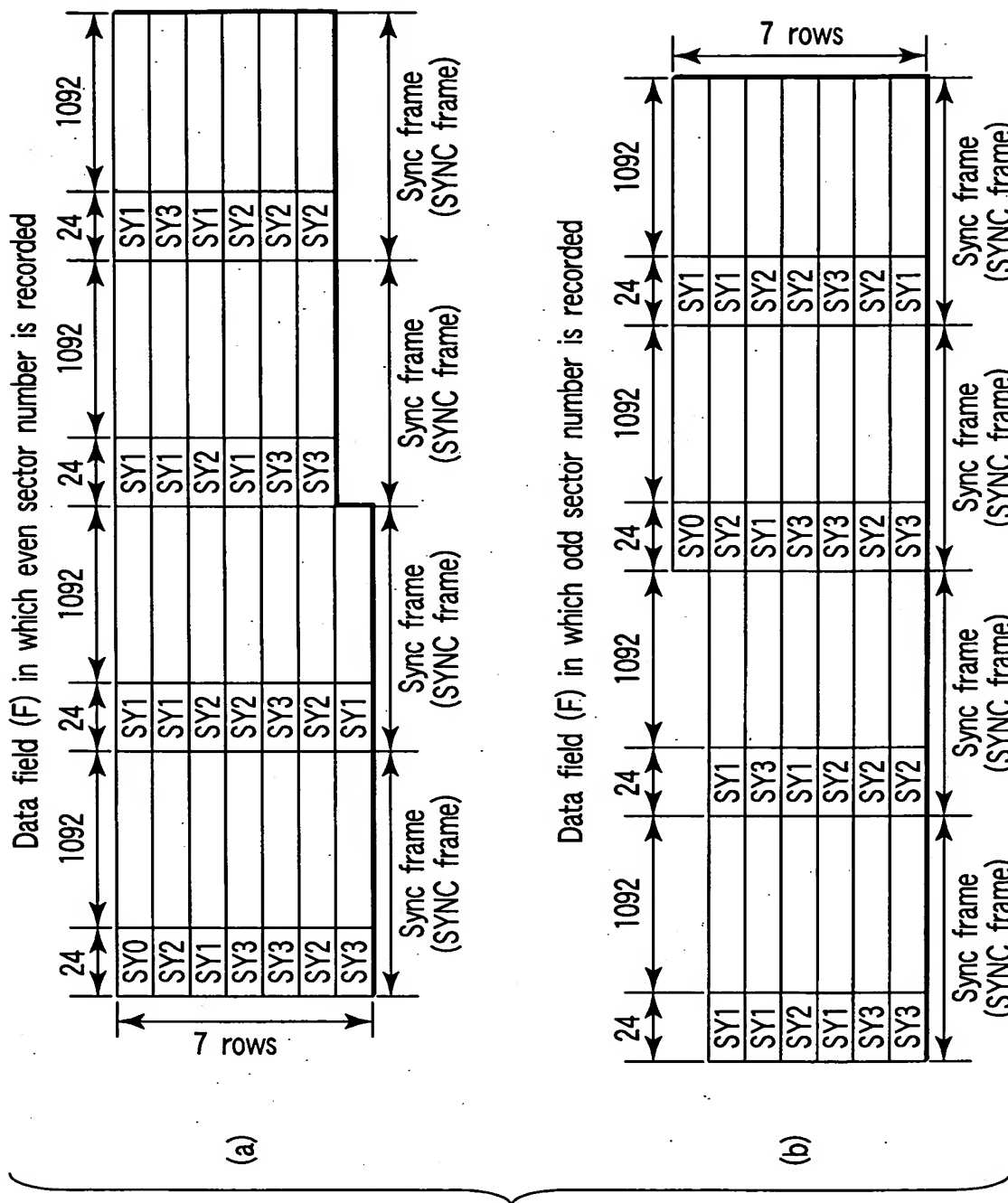


FIG. 34

Contents of specific SYNC codes

	State 0	State 1 or State 2
SY0	1000#0 01000 00000 001001	0100#0 01000 00000 001001
SY1	10100# 01000 00000 001001	00100# 01000 00000 001001
SY2	10010# 01000 00000 001001	00010# 01000 00000 001001
SY3	00000# 01000 00000 001001	00#010 01000 00000 001001

FIG. 35

Relationship between abnormal phenomena where unpredicted combination pattern of SYNC codes is detected

Contents of abnormal phenomenon→	Frame shift		Incorrect detection		Track-off
	Case 1	Case 2	Case 3	Case 4	
Contents of sense pattern ↓					Case 5
Only 1 portion is different from predicted pattern	X	○	○	X	—
With respect to excepted pattern, coincidence with pattern shifted by ±1 sync frame is obtained	○	○	X	X	X (Δ)
(1, 1, 2), (1, 2, 1), (1, 2, 2) or (2, 1, 2)	—	○	—	—	—
Continuity in data ID	(○)	(○)	○	○	X
Continuity of wobble address	(○)	(○)	○	○	X

FIG. 38

Comparison (1) of combination pattern (in column direction) of continuous SYNC codes
— In the case where code is shifted between sectors —

Newest SYNC frame number	00	01	02	03	04	05	06	07	08	09	10	11	12
Second preceding SYNC code number	2	1	0	1	1	2	1	2	2	3	1	3	3
Immediate preceding SYNC code number	1	0	1	1	2	1	2	2	3	1	3	3	1
Newest SYNC code number	0	1	1	2	1	2	2	3	1	3	3	1	2
Number of code changes between adjacent sectors	3	2	2	2	3	2	2	2	3	2	2	2	3
Number of code changes by 1 frame shift	2	2	2	1	1	2	3	2	2	2	3	3	2

Newest SYNC frame number	13	14	15	16	17	18	19	20	21	22	23	24	25
Second preceding SYNC code number	1	2	3	2	2	1	3	1	1	3	2	3	3
Immediate preceding SYNC code number	2	3	2	2	1	3	1	1	3	2	3	3	2
Newest SYNC code number	3	2	2	1	3	1	1	3	2	3	3	2	1
Number of code changes between adjacent sectors	3	2	2	2	3	2	2	2	3	2	2	2	3
Number of code changes by 1 frame shift	2	2	3	2	2	2	3	2	2	2	3	3	2

FIG. 36

Comparison (2) of combination pattern (in column direction) of continuous SYNC codes
— In the case where code is shifted between guard regions —

Newest SYNC frame number	00	01	02	03	04	05	06	07	08	09	10	11	12
Second preceding SYNC code number	1	1	0	1	1	2	1	2	2	3	1	3	3
Immediate preceding SYNC code number	1	0	1	1	2	1	2	2	3	1	3	3	1
Newest SYNC code number	0	1	1	2	1	2	2	3	1	3	3	1	2
Number of code changes between adjacent sectors	2	2	2	2	3	2	2	2	3	2	2	2	3
Number of code changes by 1 frame shift	2	2	2	1	1	2	3	2	2	2	3	3	2

Newest SYNC frame number	13	14	15	16	17	18	19	20	21	22	23	24	25	PA
Second preceding SYNC code number	1	2	3	2	2	1	3	1	1	3	2	3	3	2
Immediate preceding SYNC code number	2	3	2	2	1	3	1	1	3	2	3	3	2	1
Newest SYNC code number	3	2	2	1	3	1	1	3	2	3	3	2	1	1
Number of code changes between adjacent sectors	3	2	2	2	3	2	2	2	3	2	2	2	2	2
Number of code changes by 1 frame shift	2	2	3	2	2	2	3	2	2	2	3	3	3	2

FIG.37

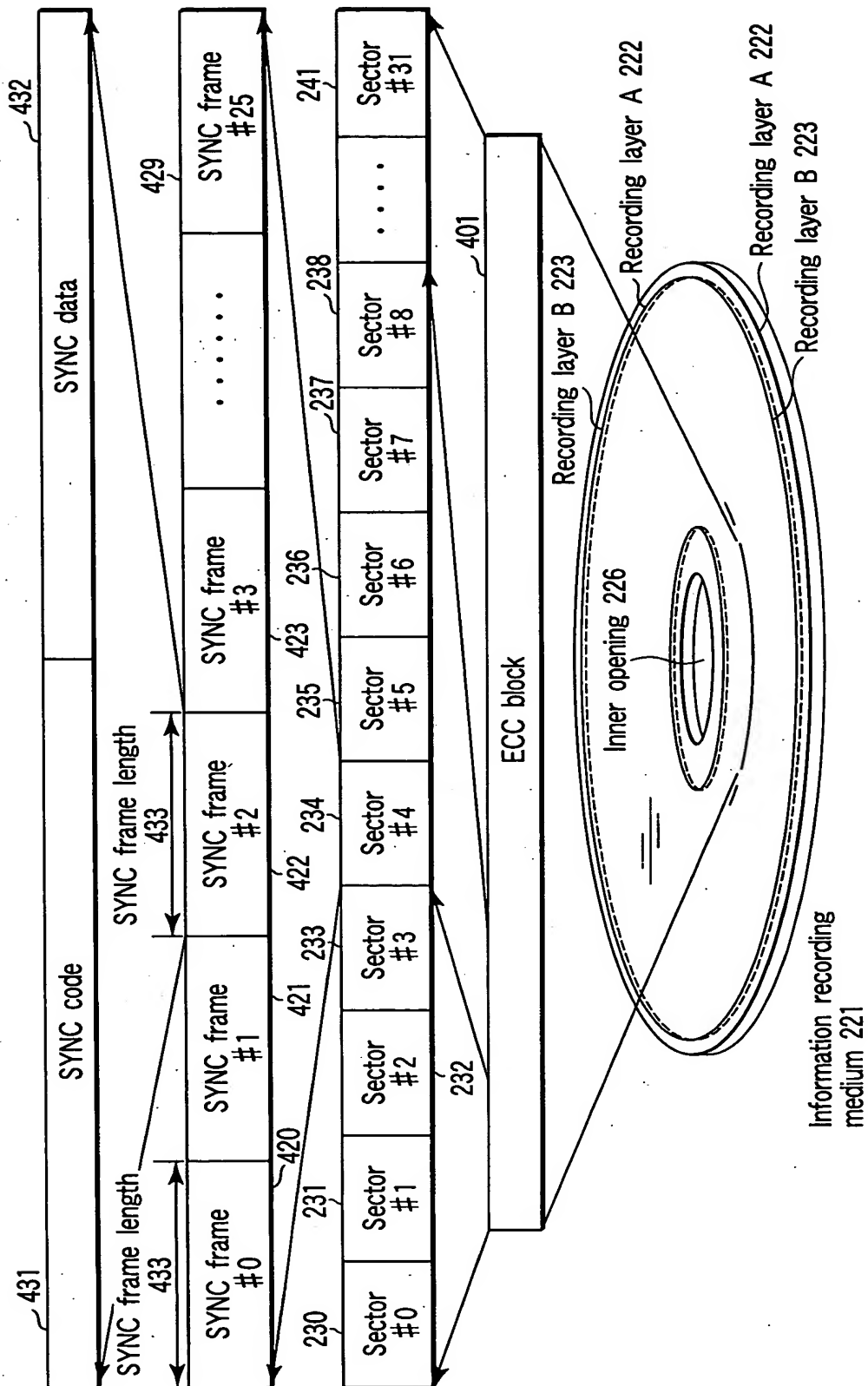


FIG. 39

Comparison between first and second embodiments in read only information recording medium

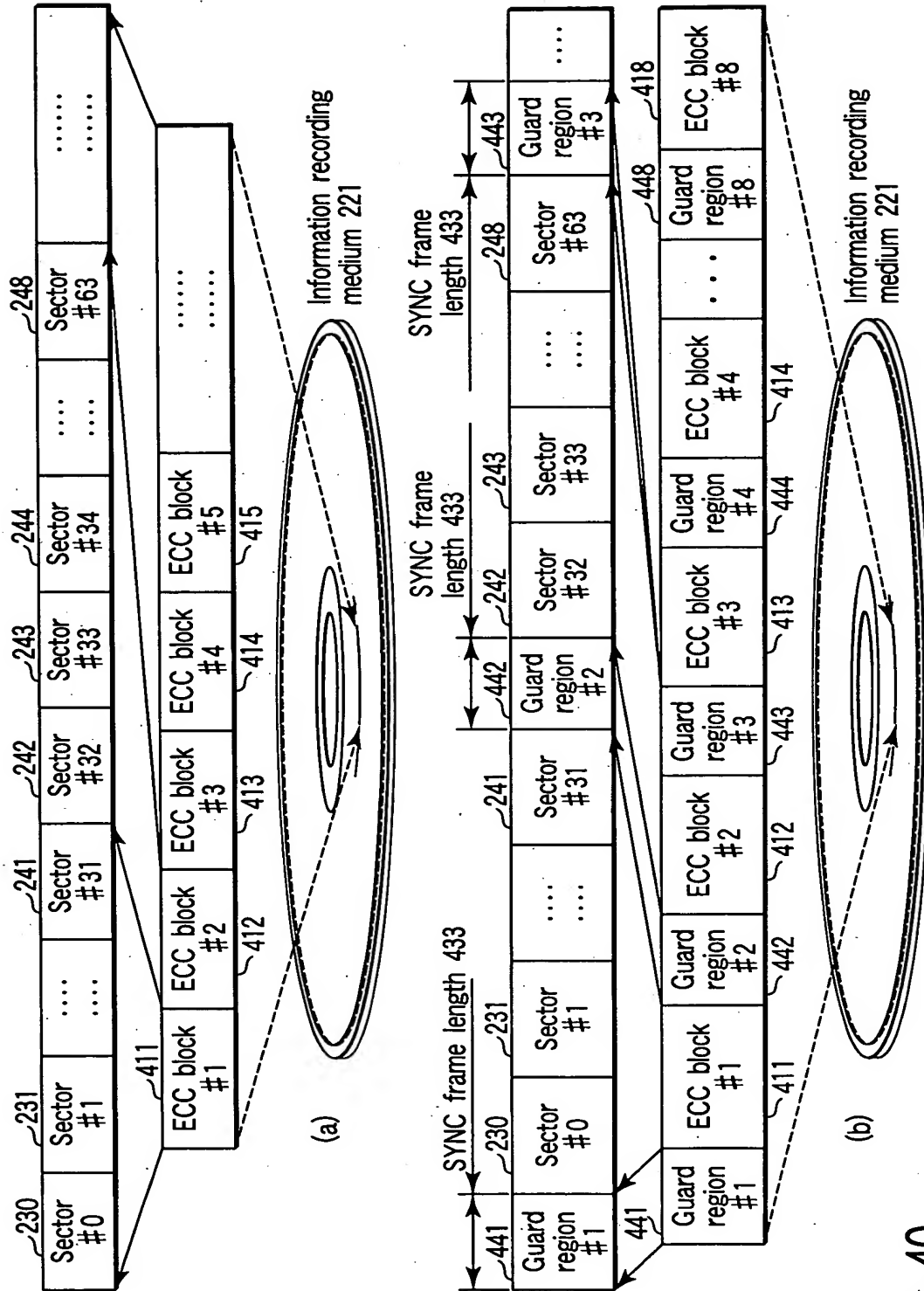


FIG. 40

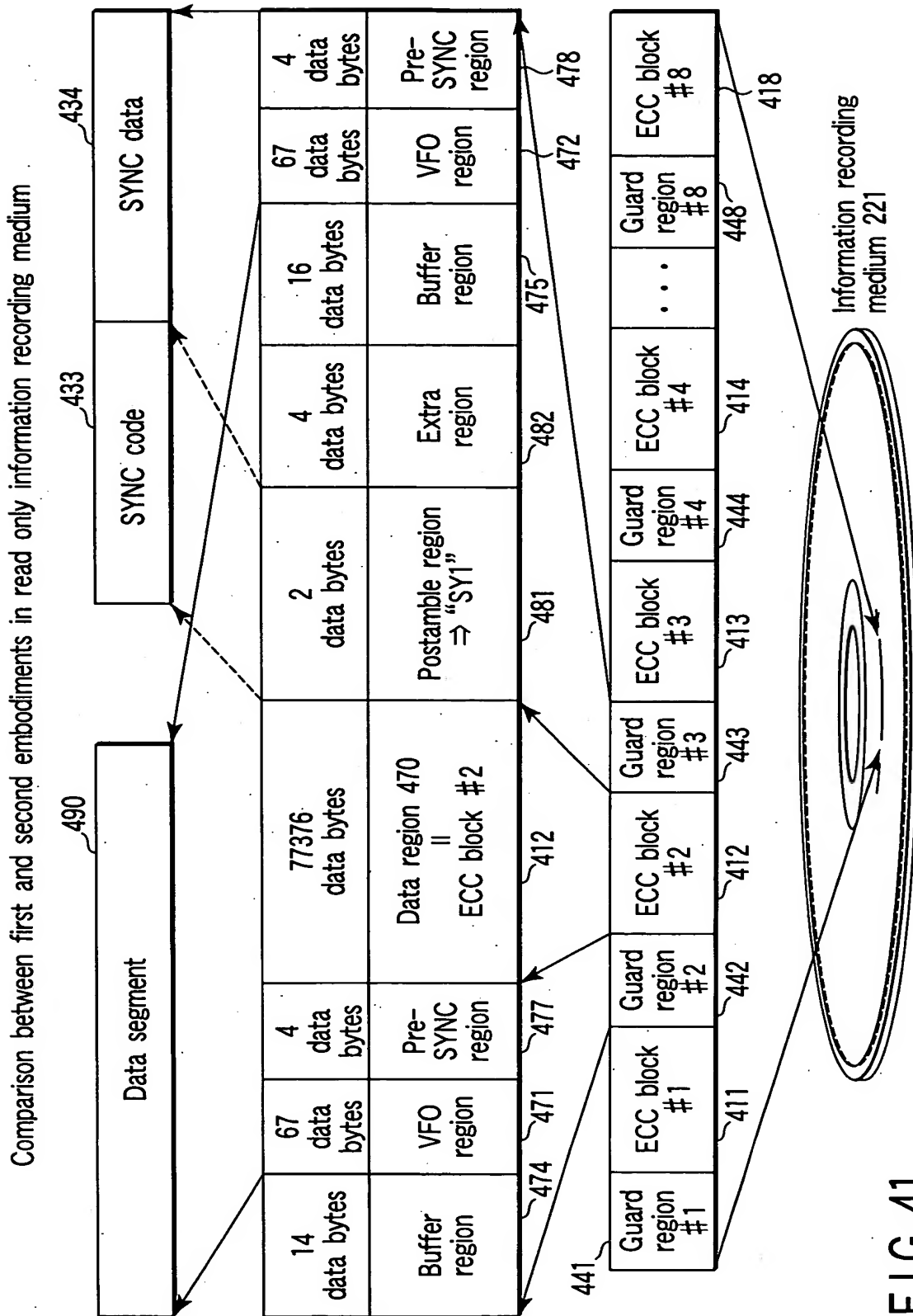


FIG. 41

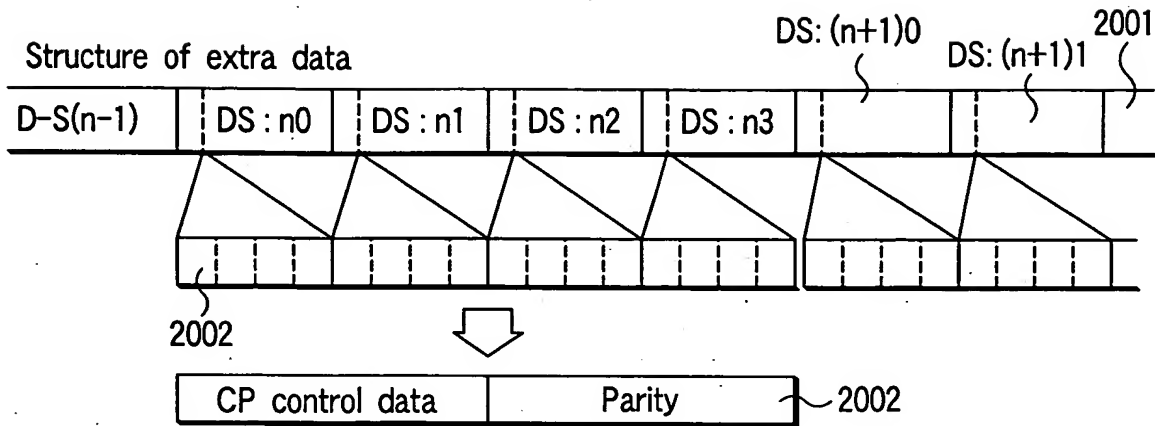


FIG. 42

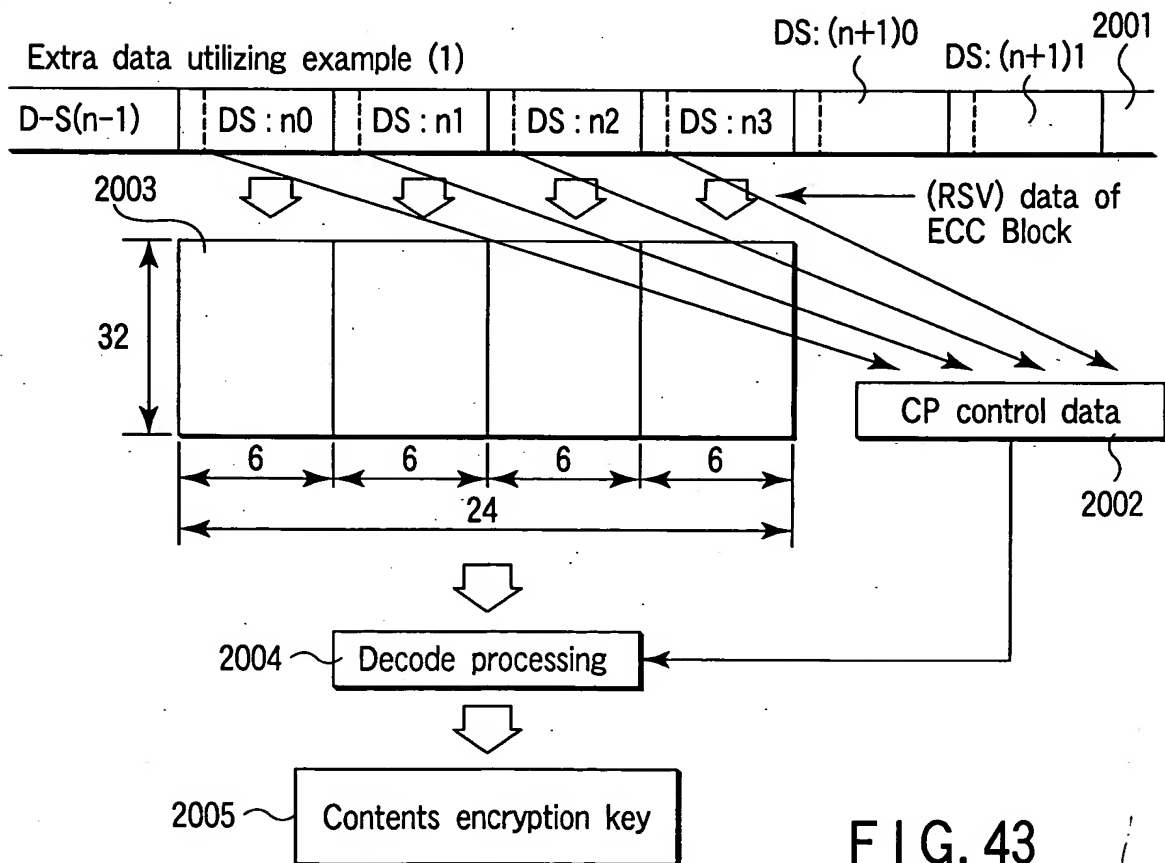


FIG. 43

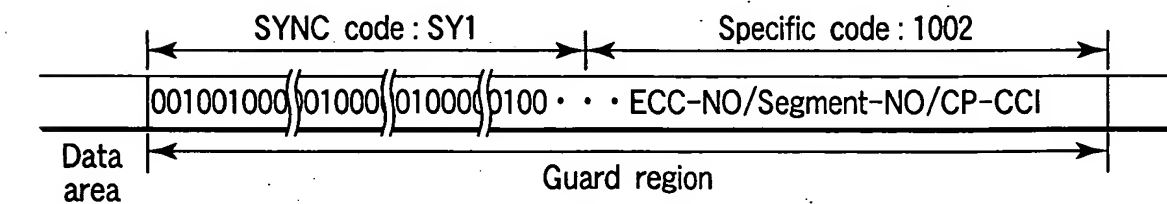
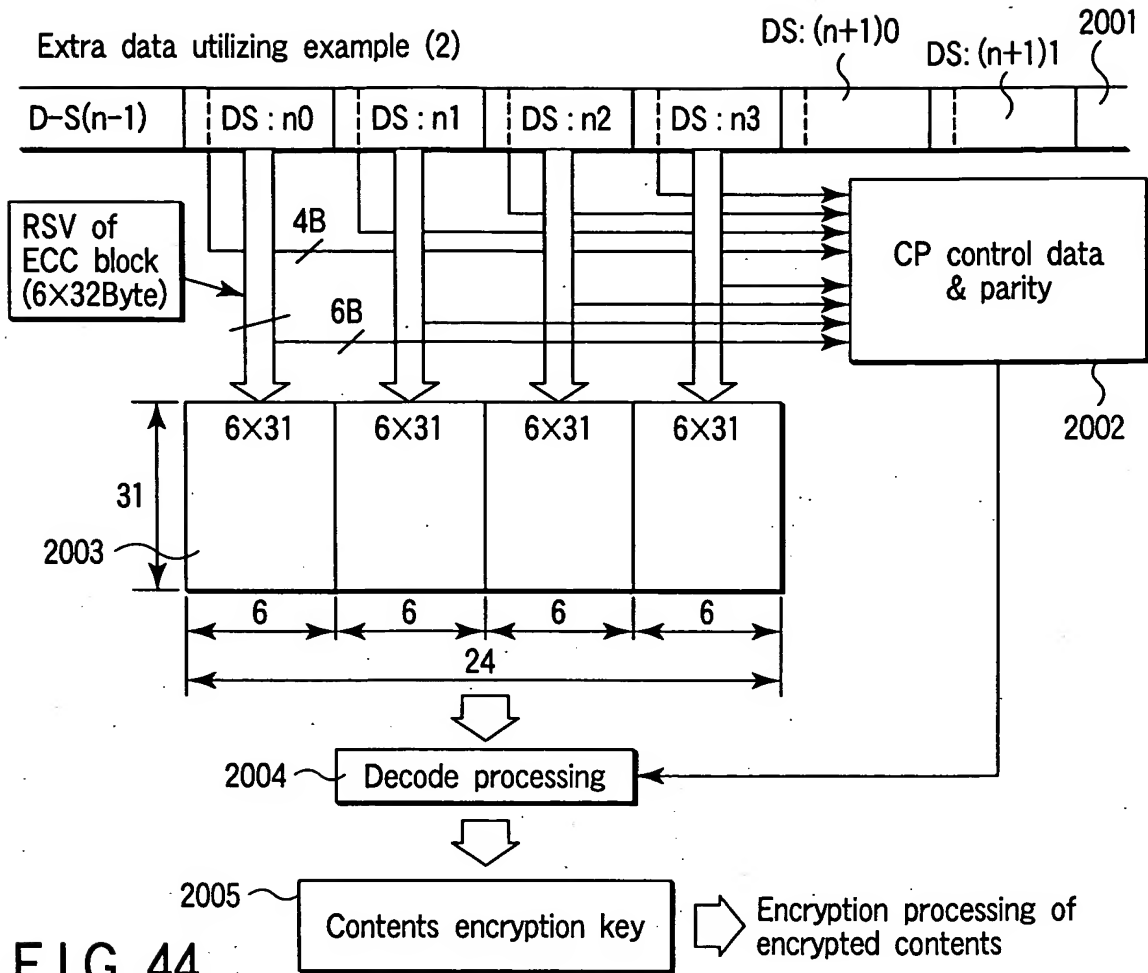


FIG. 45

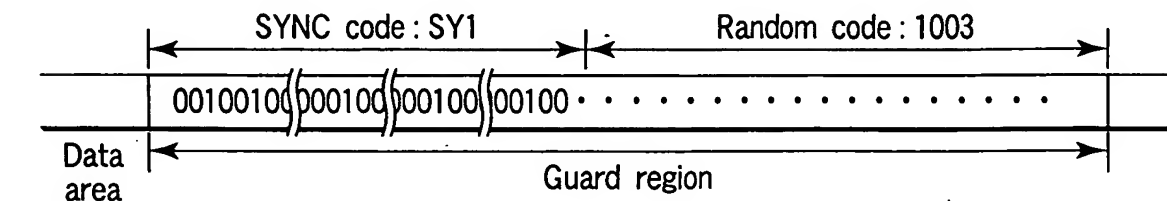


FIG. 46

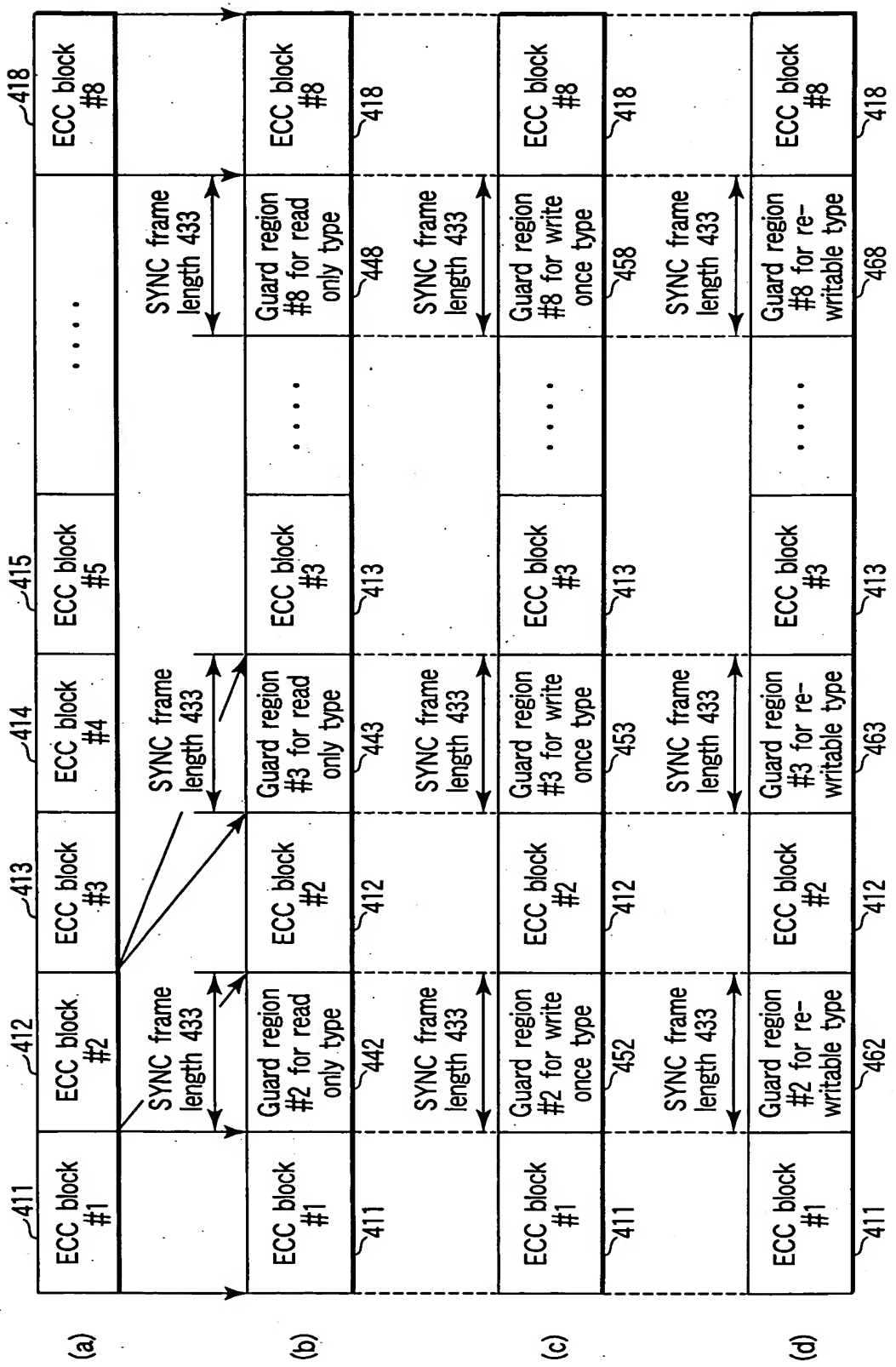


FIG. 47

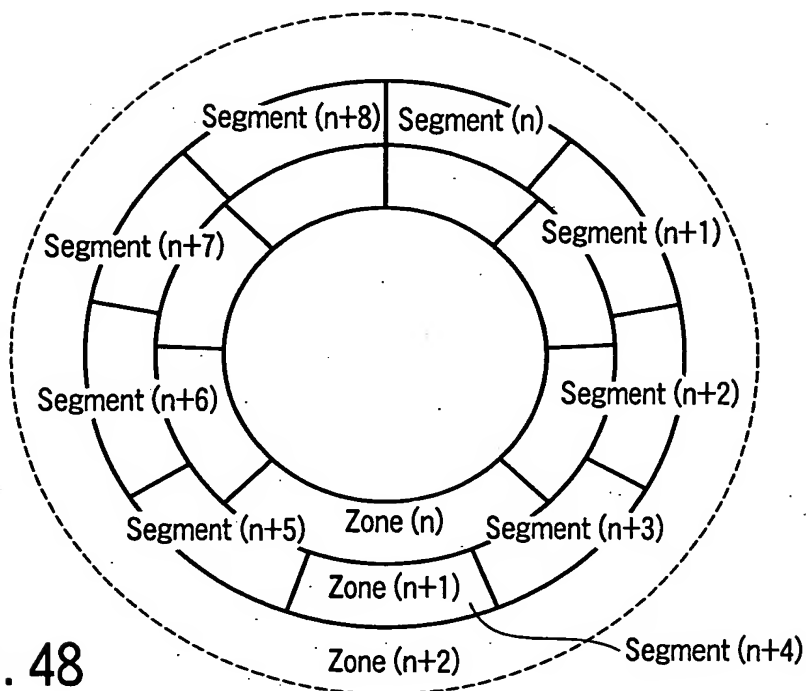
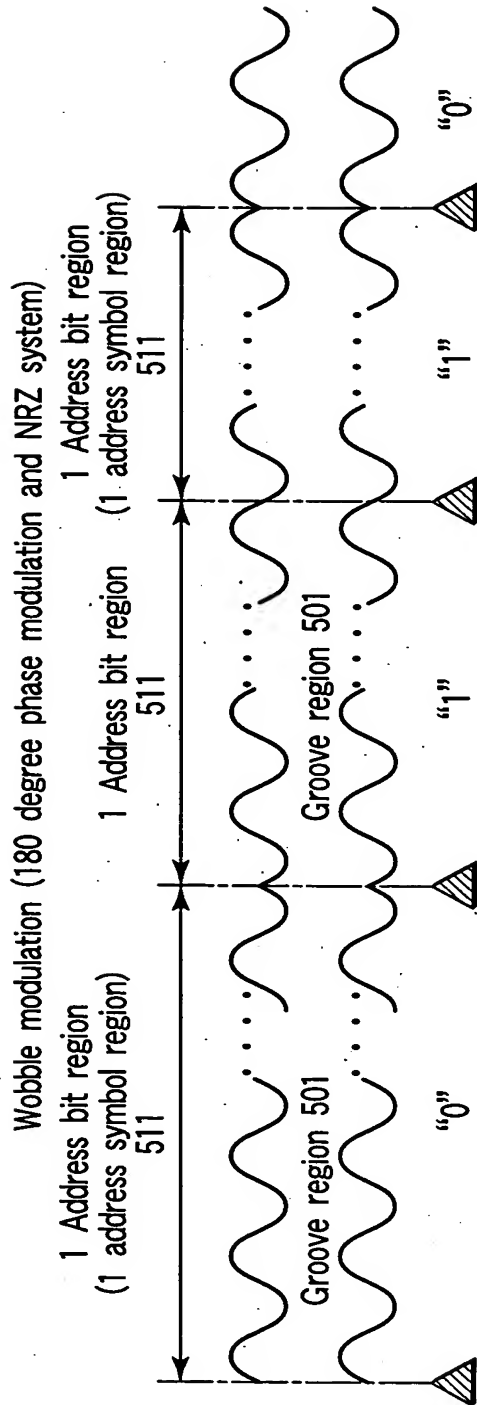


FIG. 48

Example of gray codes

Decimal notation	Conventional binary notation	Gray code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

FIG. 51



- ☆ 1 Address bit region 511 (to be expressed by 8 wobbles or 12 wobbles)
- ☆ Wobble frequency, amplitude, and phase in 1 address bit region = to be constant anywhere
- ☆ Boundary of 1 address bit region 511 (phase is shifted by 180 degrees or 0 degrees)

FIG. 49

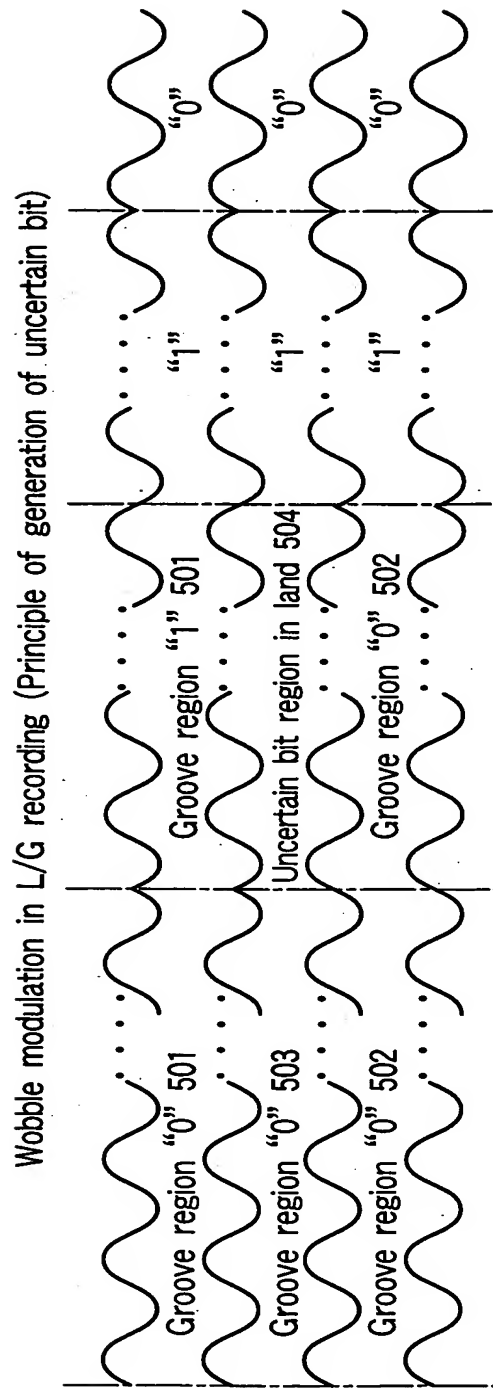


FIG. 50

Specific track code

Decimal notation	Conventional binary notation	Specific track code
0	0000	00 ... 0000
2	0010	00 ... 0001
4	0100	00 ... 0011
6	0110	00 ... 0010
8	0100	00 ... 00110
10	01010	00 ... 00111
12	01100	00 ... 00101
14	01110	00 ... 00100
16	10000	00 ... 01100
18	10010	00 ... 01101
20	10100	00 ... 01111
22	10110	00 ... 01110
24	11000	00 ... 01010
26	11010	00 ... 01011
28	11100	00 ... 01001
30	11110	00 ... 01000

Decimal notation	Conventional binary notation	Specific track code
1	00001	10 ... 00000
3	00011	10 ... 00001
5	00101	10 ... 00011
7	00111	10 ... 00010
9	01001	10 ... 00110
11	01011	10 ... 00111
13	01101	10 ... 00101
15	01111	10 ... 00100
17	10001	10 ... 01100
19	10011	10 ... 01101
21	10101	10 ... 01111
23	10111	10 ... 01110
25	11001	10 ... 01010
27	11011	10 ... 01011
29	11101	10 ... 01001
31	11111	10 ... 01000

Note: "2n" (n: Integer value) and "2n+1" are different from each other only in the most significant bit, and are all the same in other bits

FIG. 52

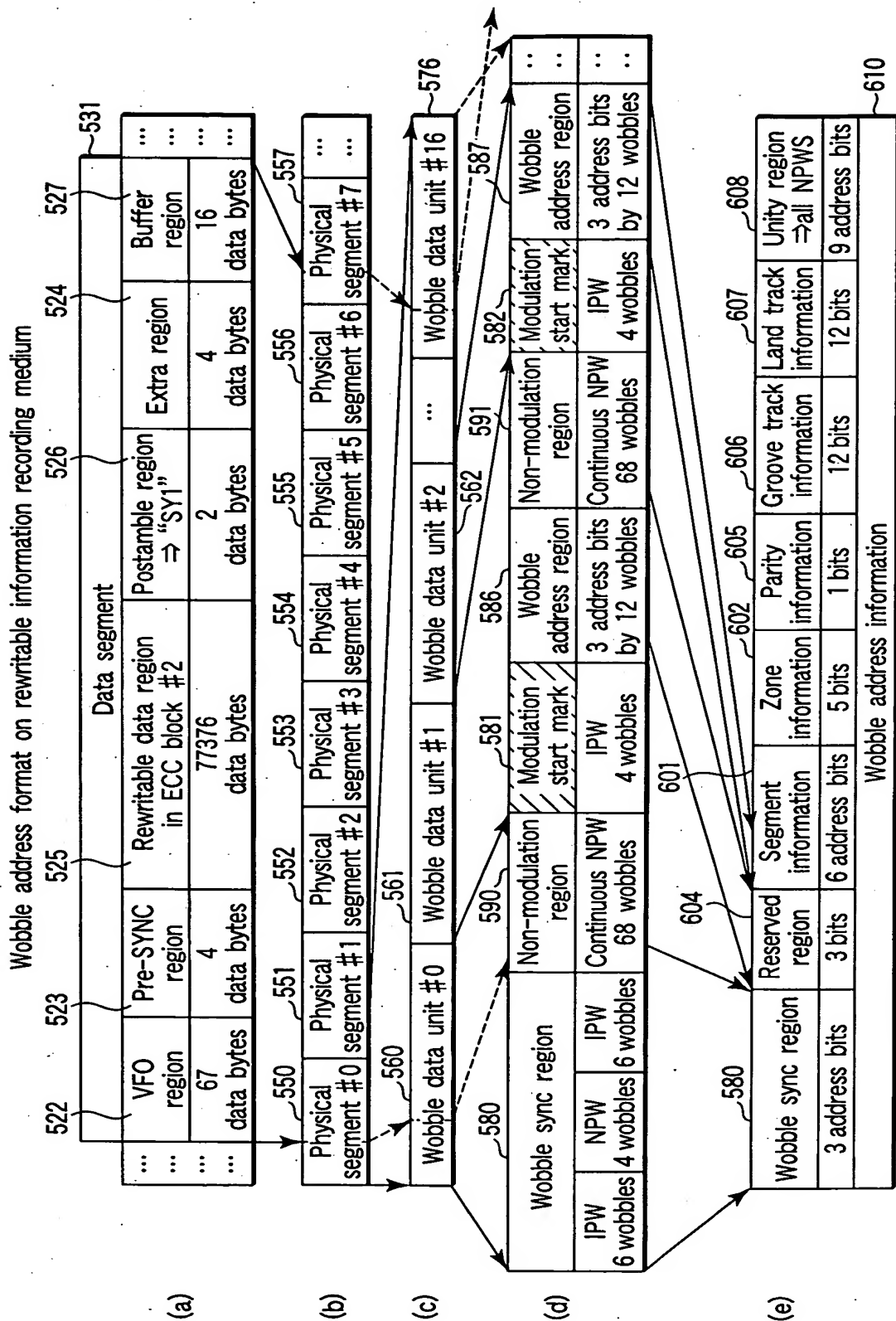


FIG. 53

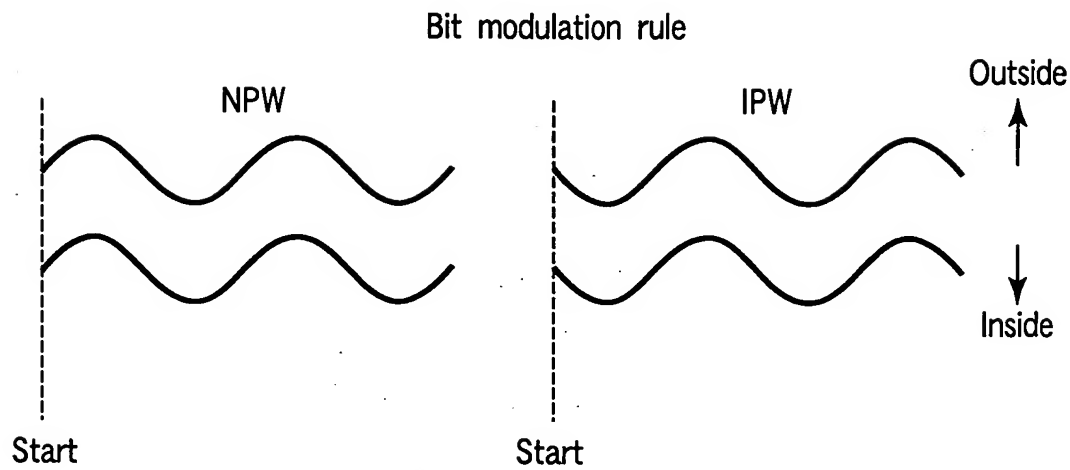


FIG. 54

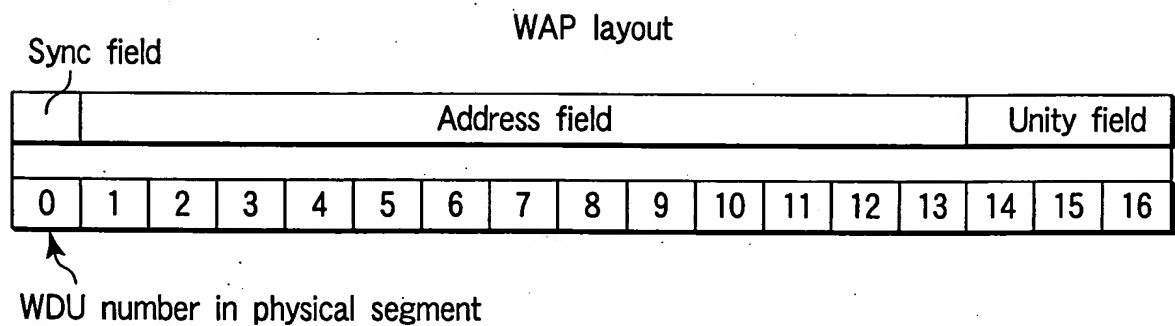


FIG. 55

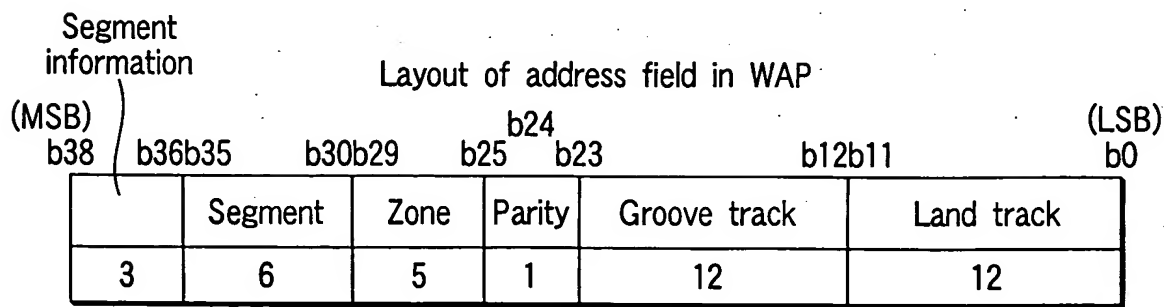


FIG. 56

Binary/gray code conversion

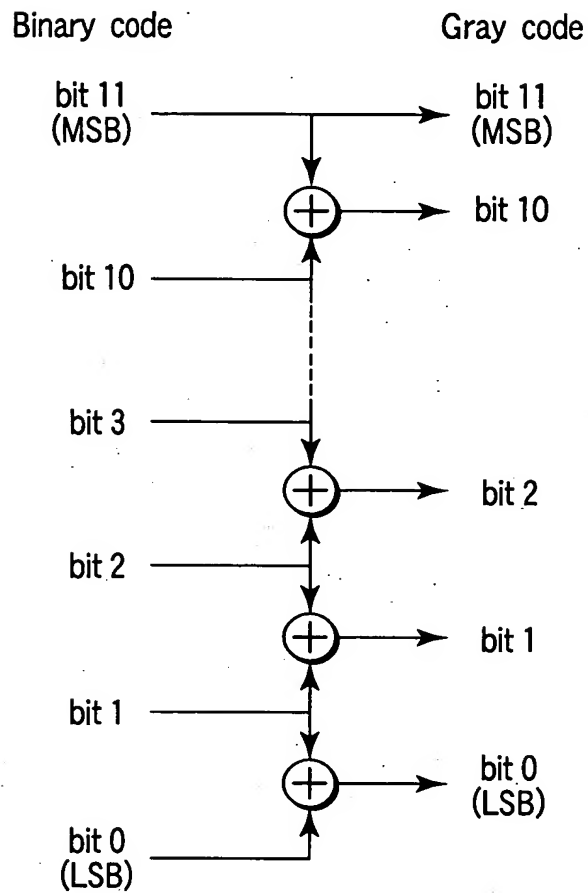


FIG. 57

WDU in sync field

SYNC	IPW	NPW	IPW	NPW
	6 wobbles	4 wobbles	6 wobbles	68 wobbles

FIG. 58

WDU in address field

Address	IPW	bit 2	bit 1	bit 0	NPW
	4 wobbles	4 wobbles	4 wobbles	4 wobbles	68 wobbles

FIG. 59

WDU in unity field

Unity	NPW
	84 wobbles

FIG. 60

WDU of outside mark

NPW	SCM 1	NPW	SCM 2	NPW	NPW
		8 wobbles			68 wobbles
2 wobbles	2 wobbles		2 wobbles	2 wobbles	

FIG. 61

内側マークのWDU

NPW	SCM 1	NPW	SCM 2	NPW	NPW
		4 wobbles		6 wobbles	68 wobbles
2 wobbles	2 wobbles		2 wobbles		

FIG. 62

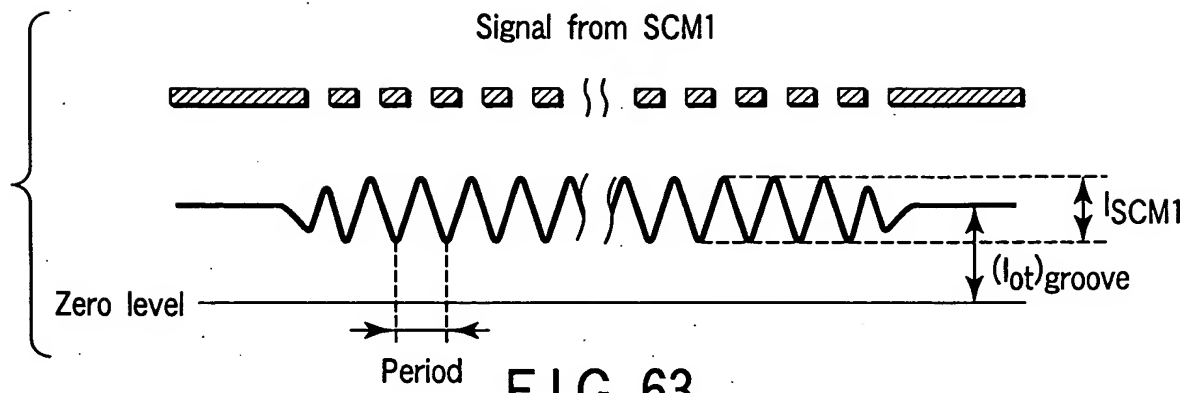


FIG. 63

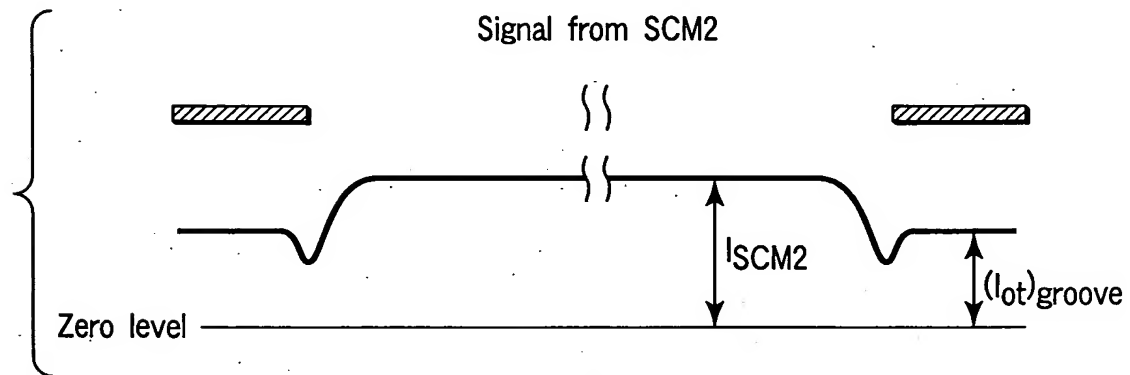


FIG. 64

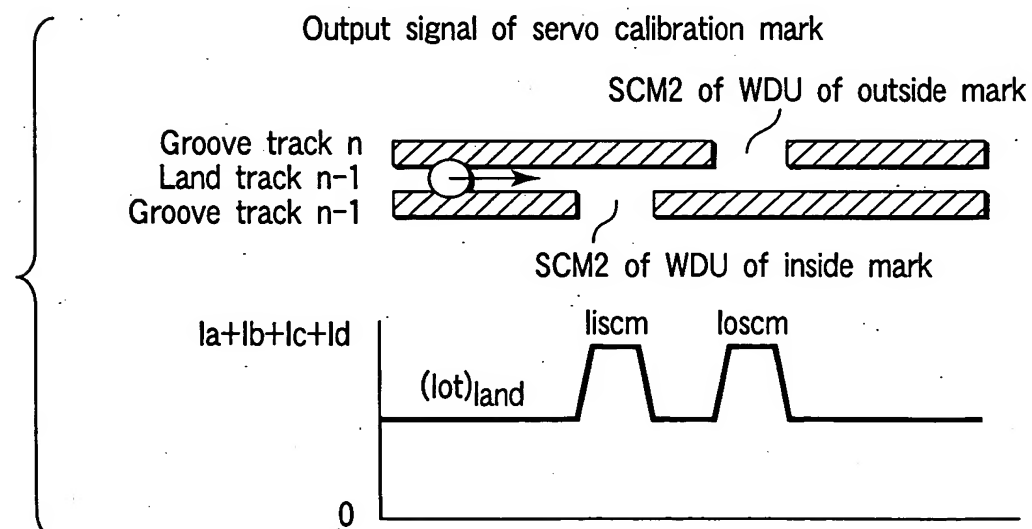
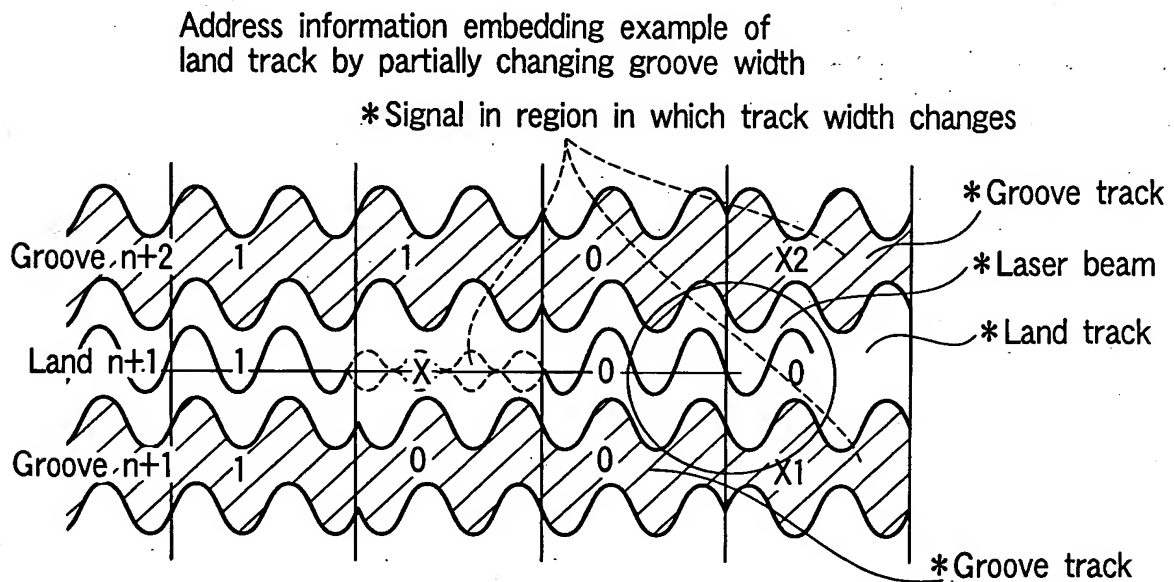
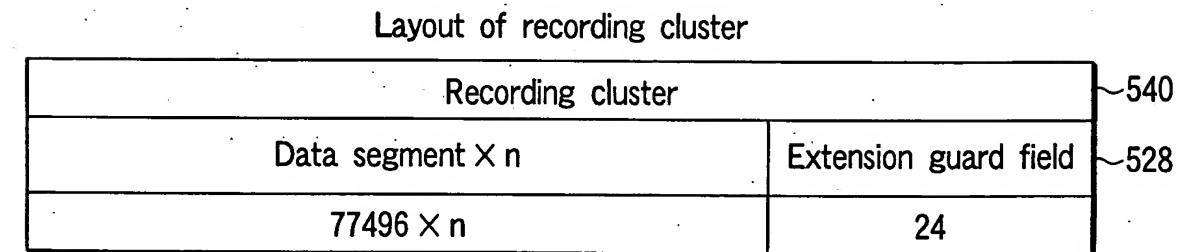
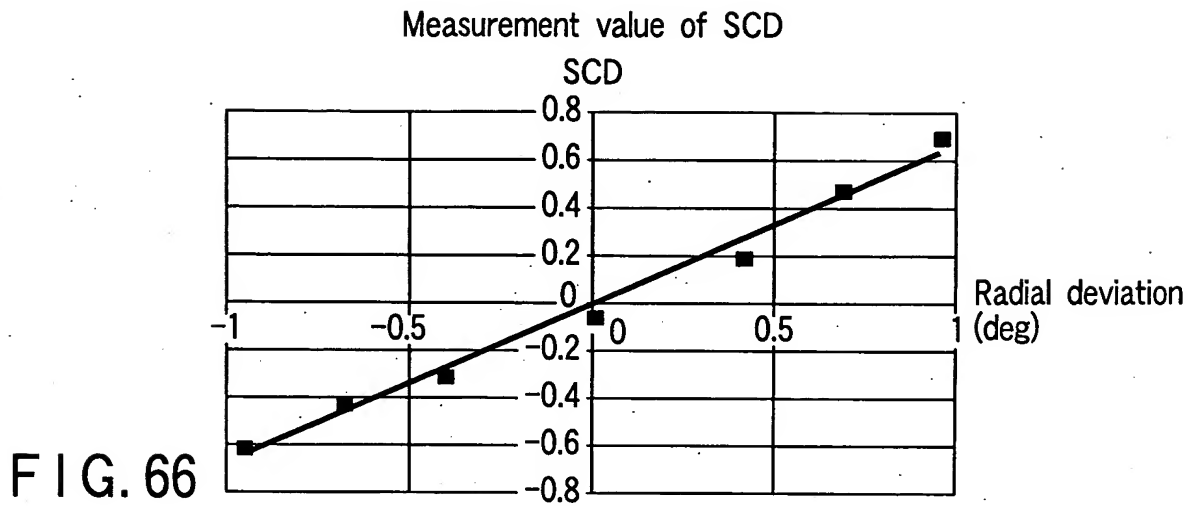


FIG. 65



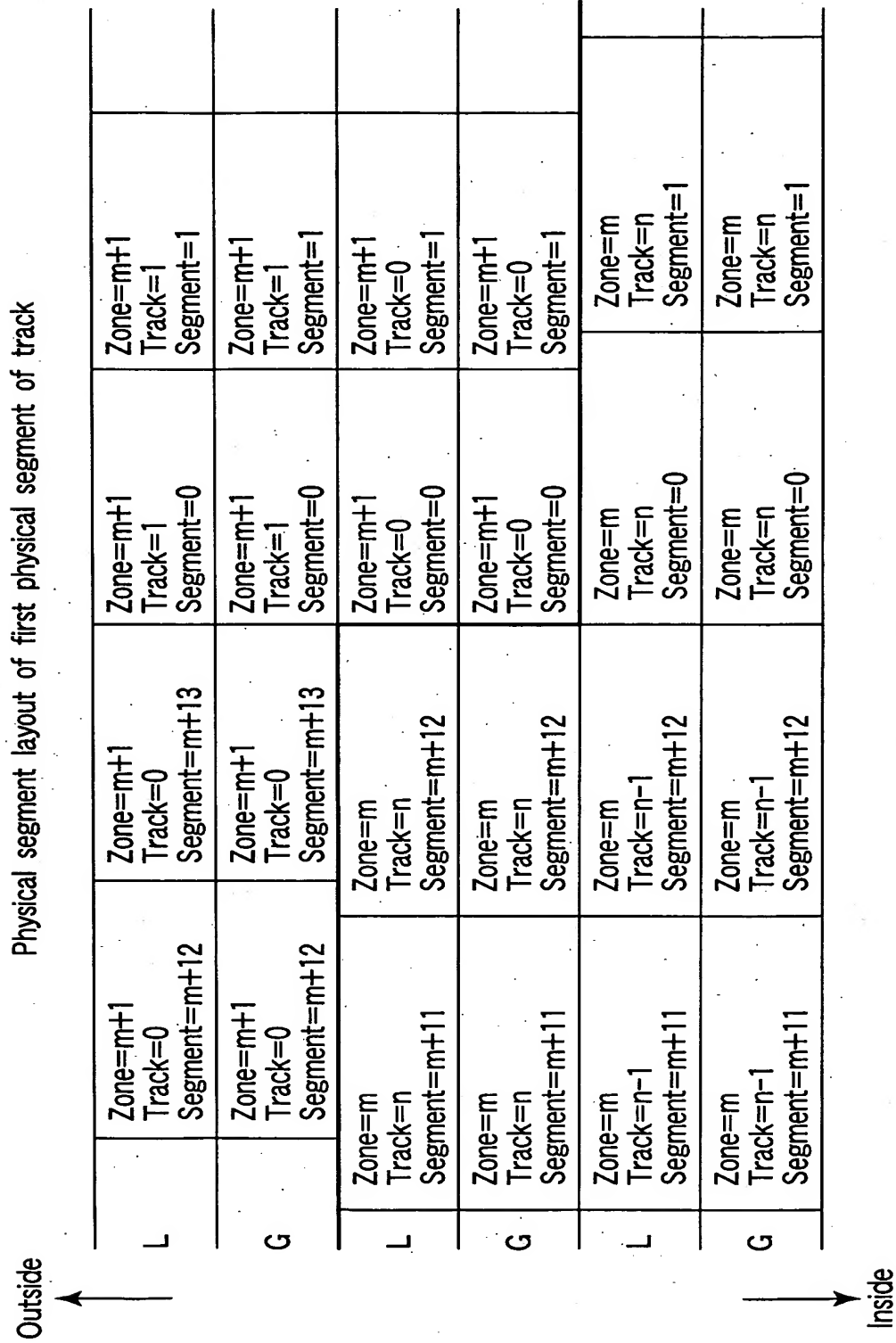


FIG. 67

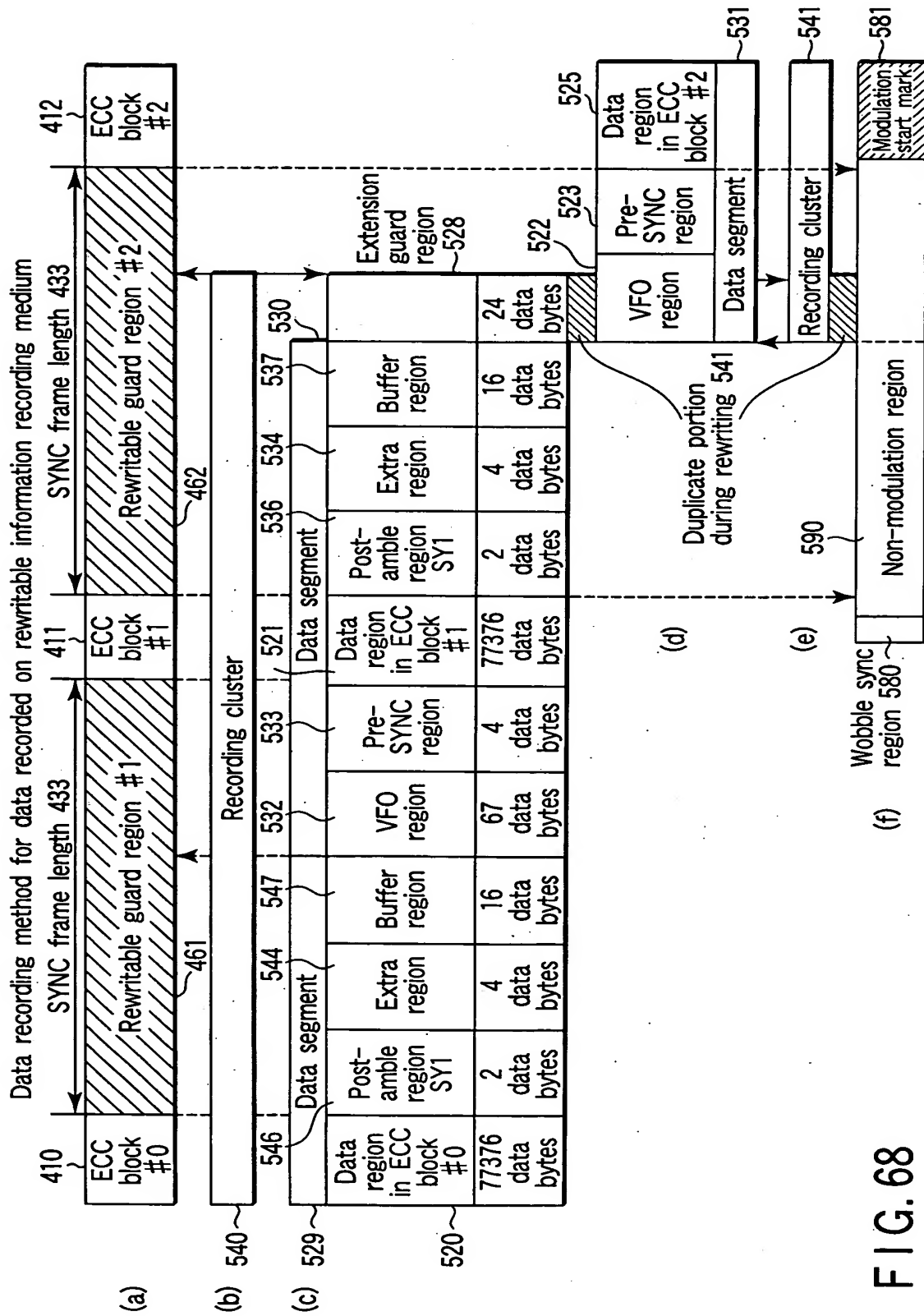


FIG. 68

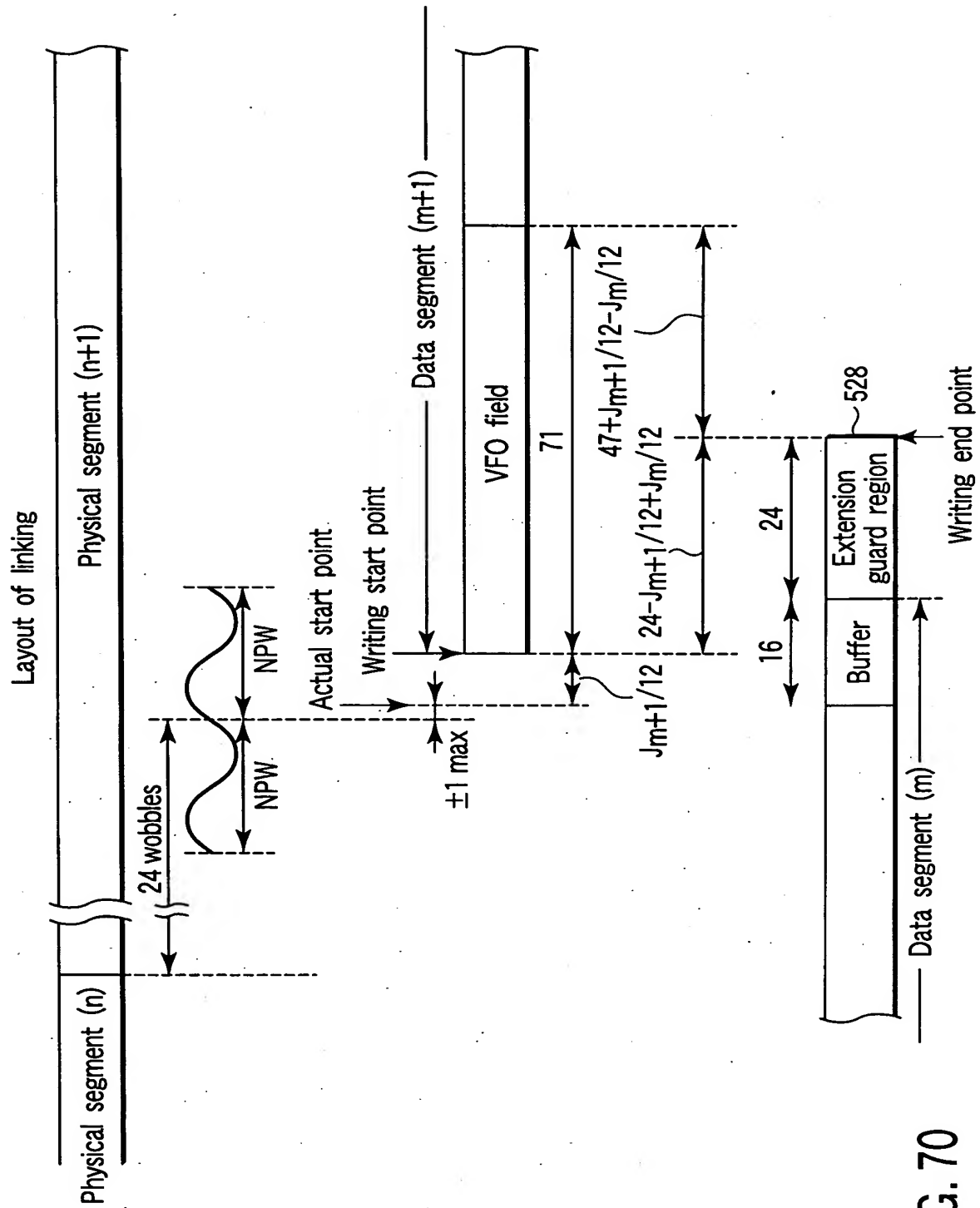


FIG. 70

Example wherein land address is formed by partially changing groove width

Groove track	G-S 1101	L-S 11X1	G-S 1101	L-S 11X1	
Land track		L-S 1101		L-S 1100	
Groove track	G-S 1100	L-S X100	G-S 1100	L-S X100	
Land track		L-S 0101		L-S 0100	
Groove track	G-S 0101	L-S 010X	G-S 0100	L-S 010X	

FIG. 72

Example wherein odd number or even number of land track is detected by partially changing groove width

Groove/land track	Track number	Criterion for determining track number
Groove : G(n+2)	1101X	For groove, first 4 bits only are valid
Odd land : L(n+1)	110X0	Either 11010 or 11000 is valid only in this field in odd land
Groove : G(n+1)	1100X	For groove, first 4 bits only are valid
Even land : L(n)	X1001	Either 11001 or 01001 is valid only in this field in even land
Groove : G(n)	0100X	For groove, first 4 bits only are valid

FIG. 73

Another example wherein uncertain bit is allocated in groove region
in land/groove recording

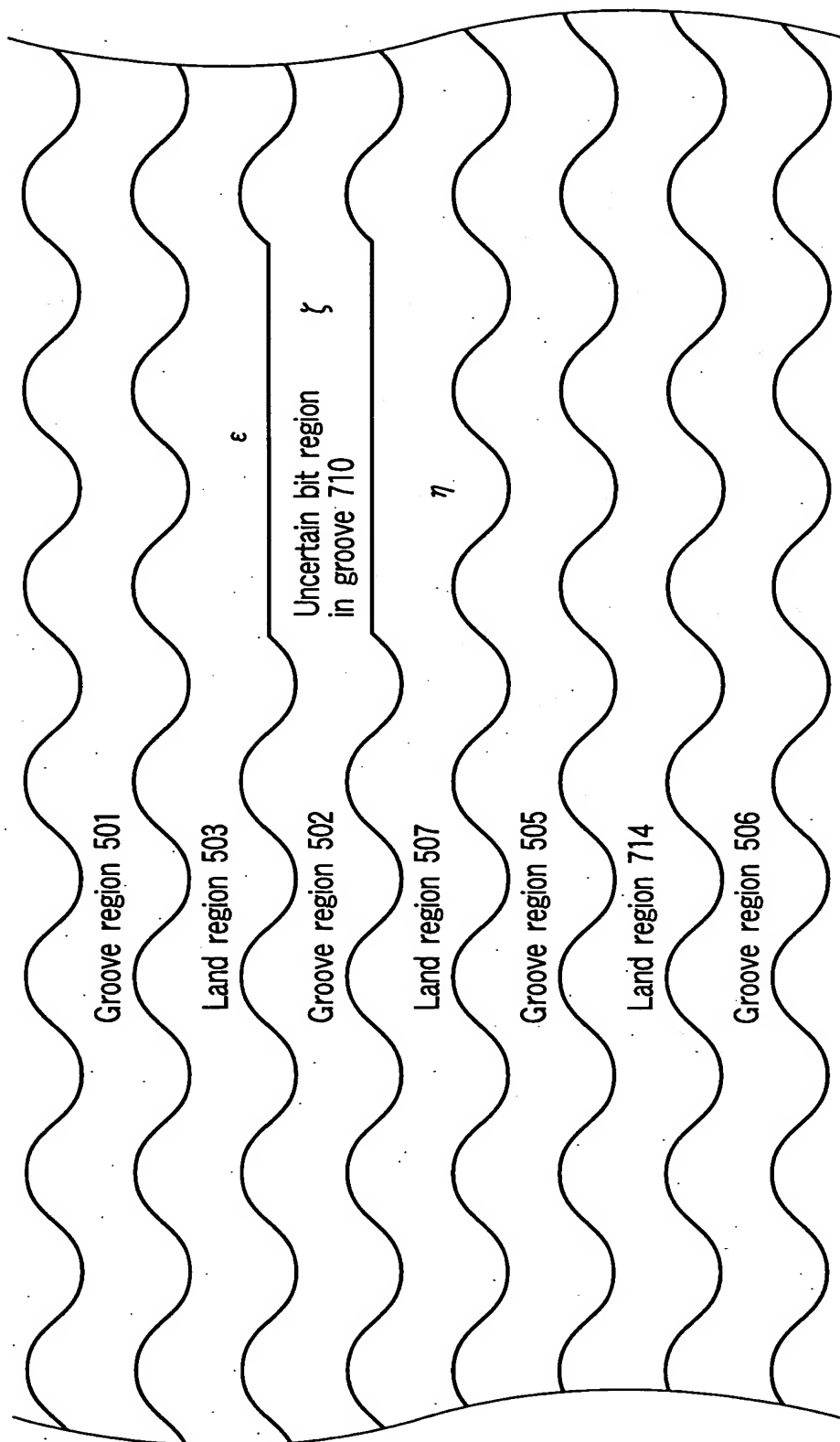


FIG. 74

Rewritable information recording medium (method for setting track number information)

Land or groove identification	Track number	Track number information A606	Track number information B607
Groove	2n+3	2n+4	2n+3
Land	2n+3	Uncertain (2n+2 or 2n+3)	2n+3
Groove	2n+2	2n+2	2n+3
Land	2n+2	2n+2	Uncertain (2n+1 or 2n+3)
Groove	2n+1	2n+2	2n+1
Land	2n+1	Uncertain (2n or 2n+2)	2n+1
Groove	2n	2n	2n+1

FIG. 75

Wobble detection signal in land track

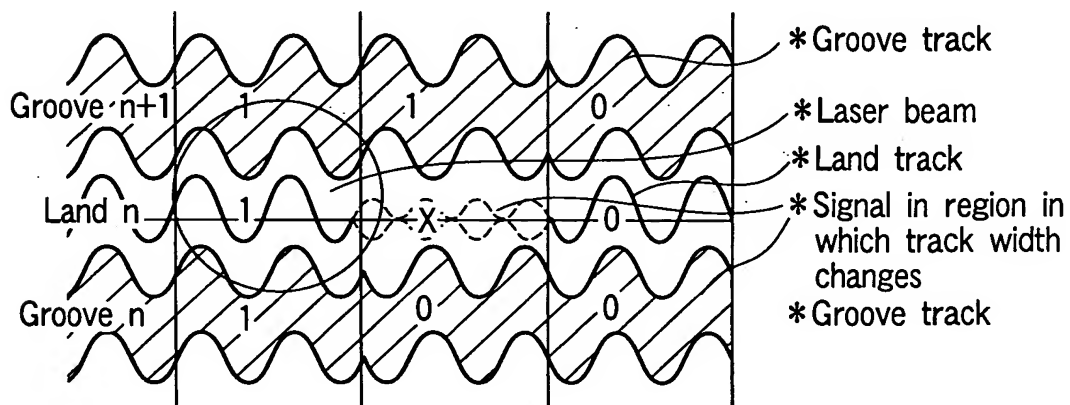


FIG. 76

Relationship between address detection
values in land track in groove wobbling

Track mode	Track number to be detected
Groove	$n+3$
Even land ($n+2$)	$(n+2)$ or $(n+3)$
Groove	$n+2$
Even land ($n+1$)	$(n+1)$ or $(n+2)$
Groove	$n+1$
Even land (n)	(n) or $(n+1)$
Groove	n

FIG. 77

Track number by groove wobbling
and detection data in land track

Groove/land track	Track number	Criterion for determining track number
Groove : $G(n+2)$	1101	
Odd land : $L(n+1)$	110*	1101 or 1100 is valid only in this field in odd land
Groove : $G(n+1)$	1100	
Even land : $L(n)$	*100	1100 or 0100 is valid only in this field in even land
Groove : $G(n)$	0100	

FIG. 78

Example of addressing format in rewritable information recording medium

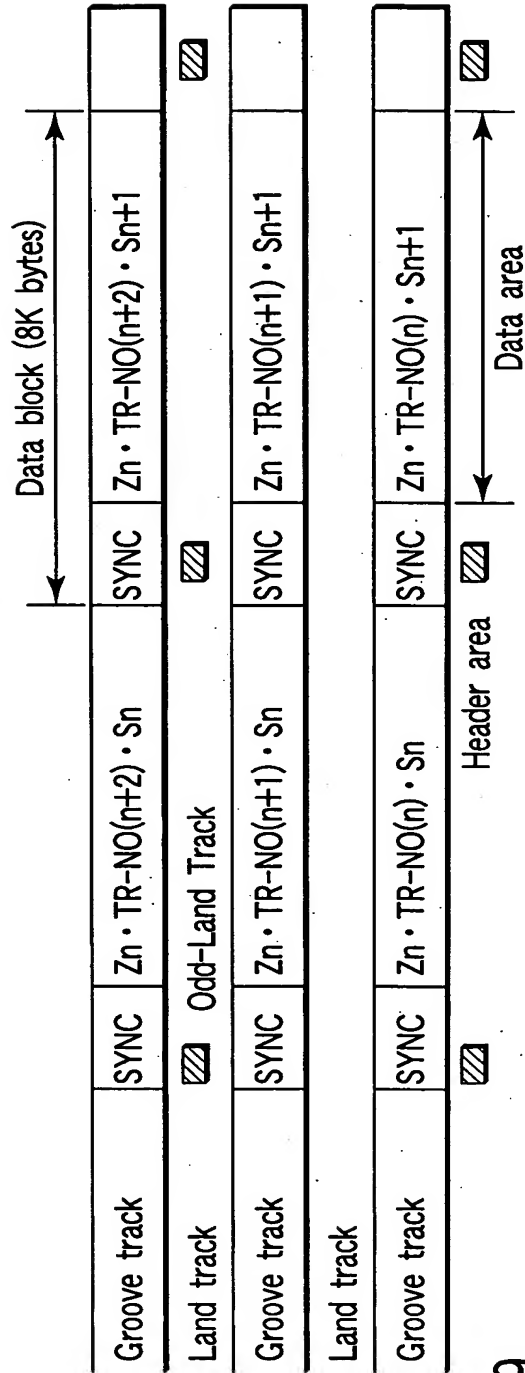


FIG. 79

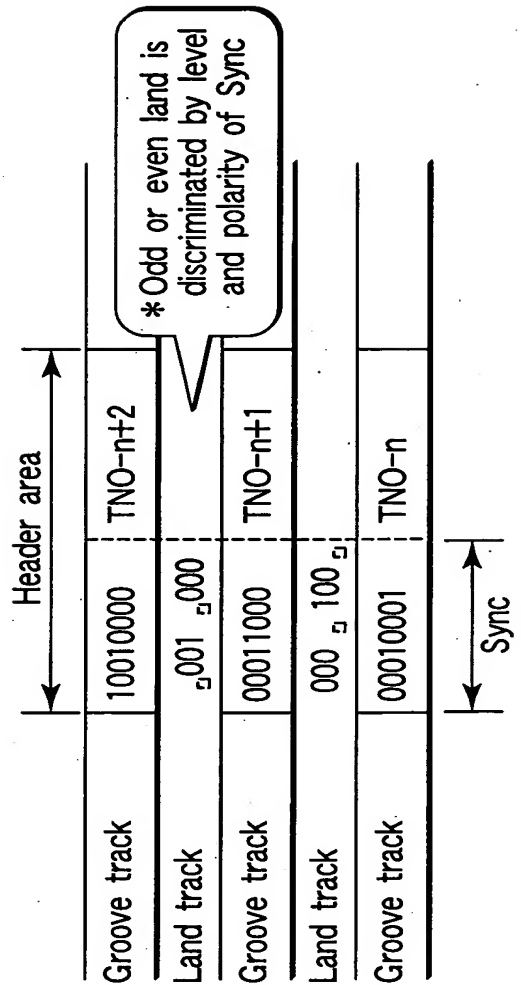


FIG. 80

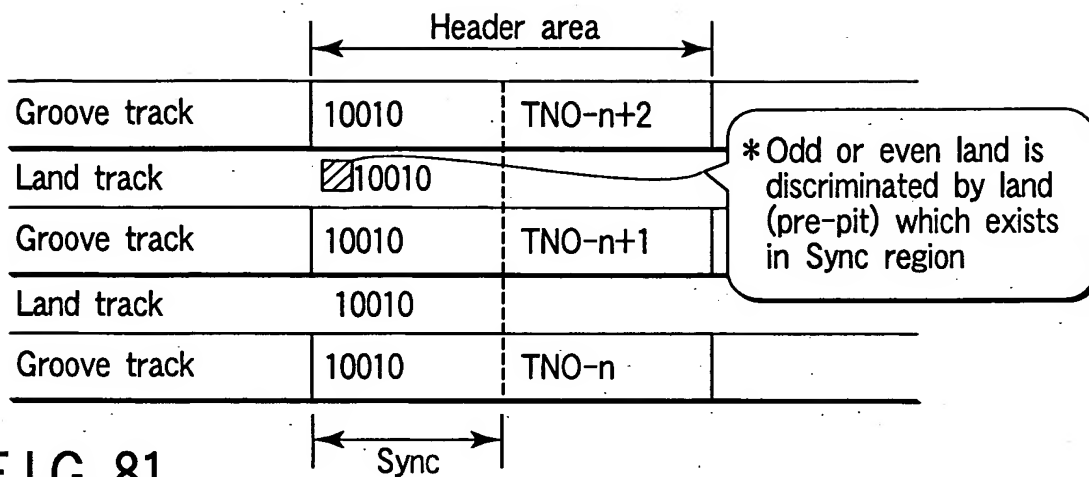


FIG. 81

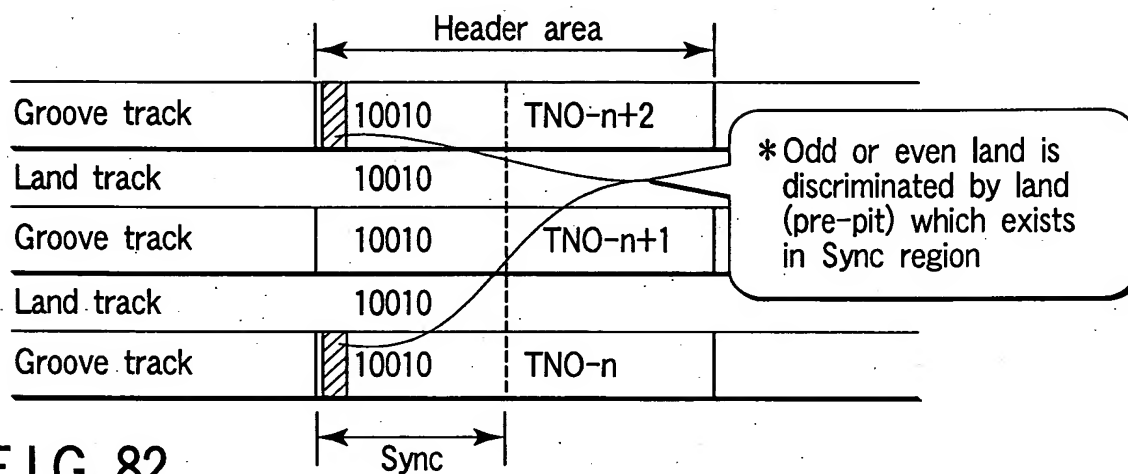


FIG. 82

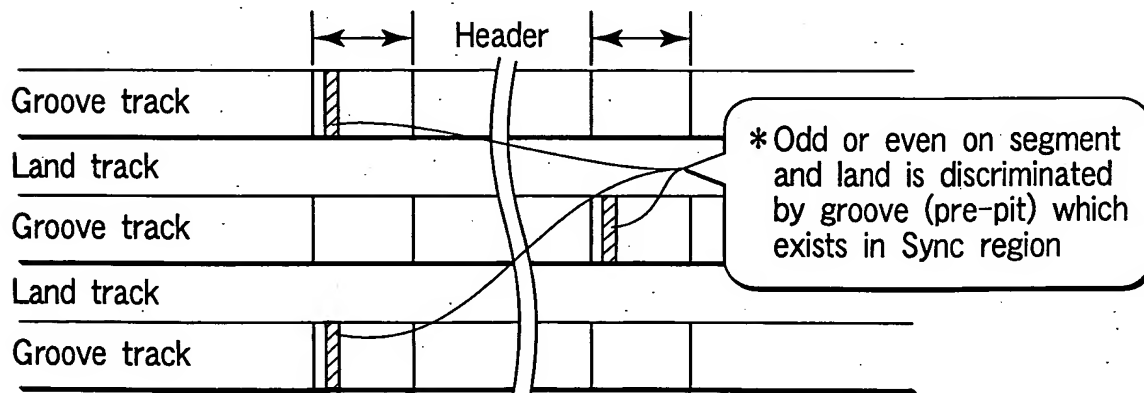


FIG. 83

Land or groove recording
(method for setting odd or even number identification information on land)

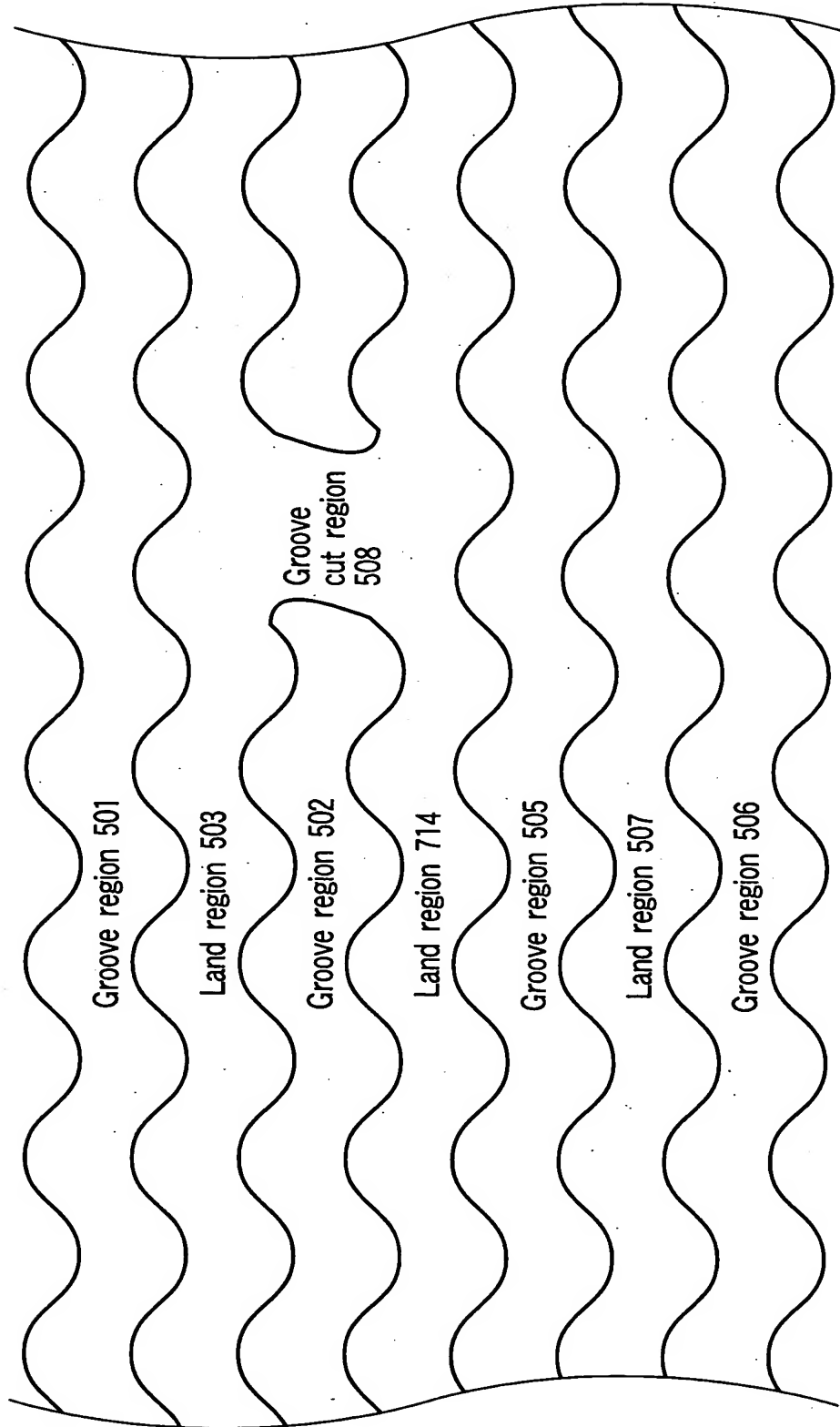


FIG. 84

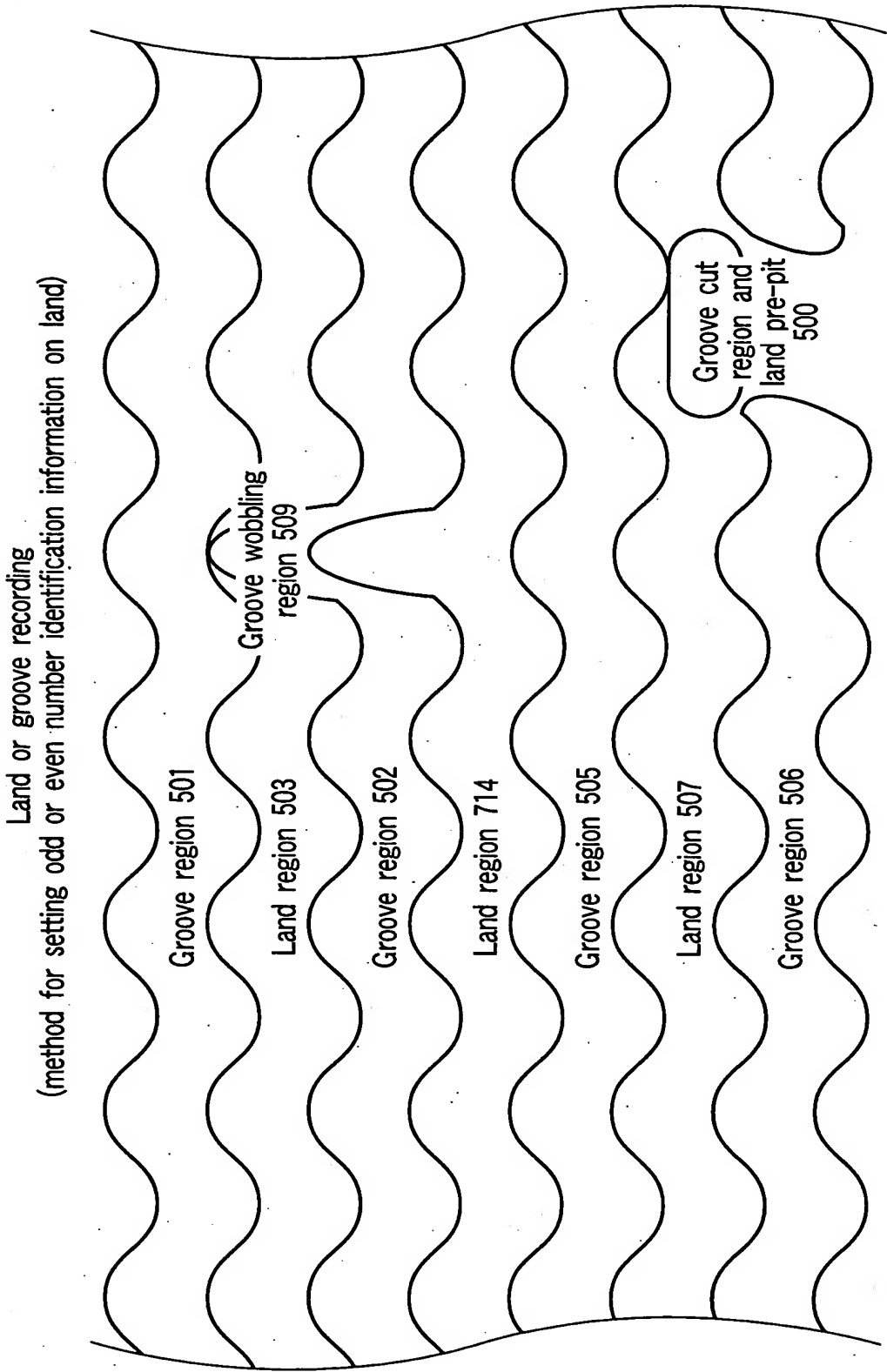


FIG. 85

Dimensional comparison table between system lead-in area and current DVD-ROM

Information recording medium	Single layer disk		Dual layer disk	
	Track pitch	Shortest pit length	Track pitch	Shortest pit length
Embodiment of the invention	0.68 μm	0.41 μm	0.68 μm	0.41 μm
Value defined in current DVD-ROM	0.74 μm	0.40 μm	0.74 μm	0.44 μm
Ratio of the embodiment of the invention to value defined in the current DVD-ROM	0.92	1.03	0.96	1.07
Allowable upper limit of the present invention (1.3 times as high as value defined in the current DVD-ROM)	0.96 μm	0.52 μm	0.96 μm	0.57 μm
Allowable lower limit of the present invention (0.7 times as low as value defined in the current DVD-ROM)	0.52 μm	0.28 μm	0.52 μm	0.31 μm

FIG. 86

Data structure of lead-in area in read only information recording medium

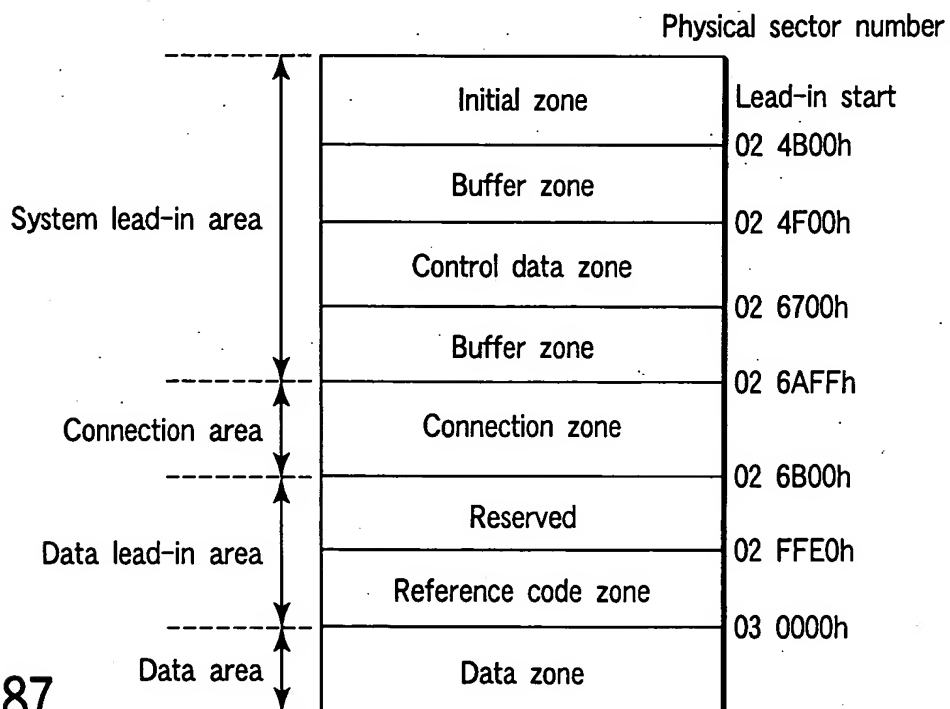


FIG. 87

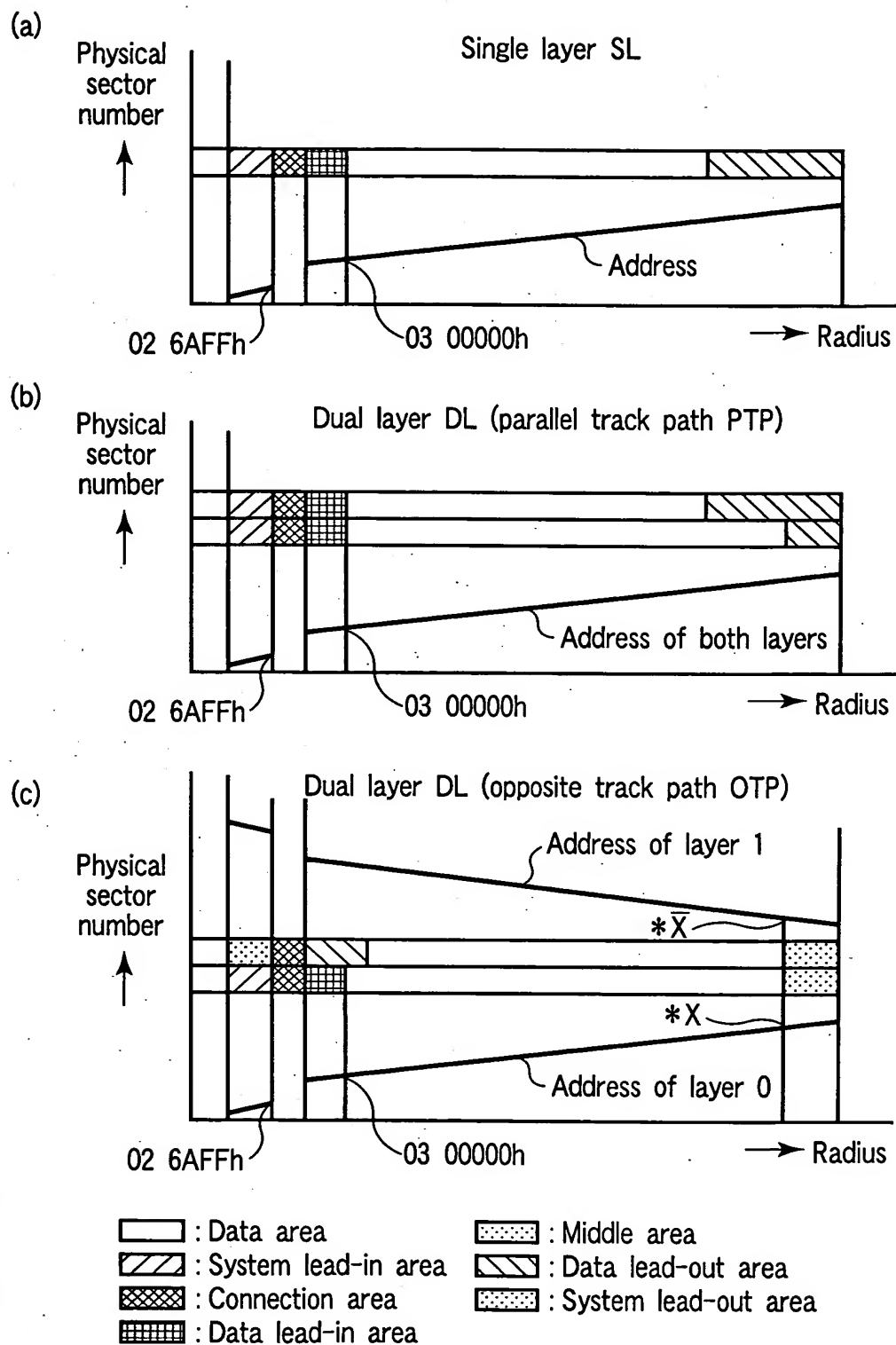


FIG. 88

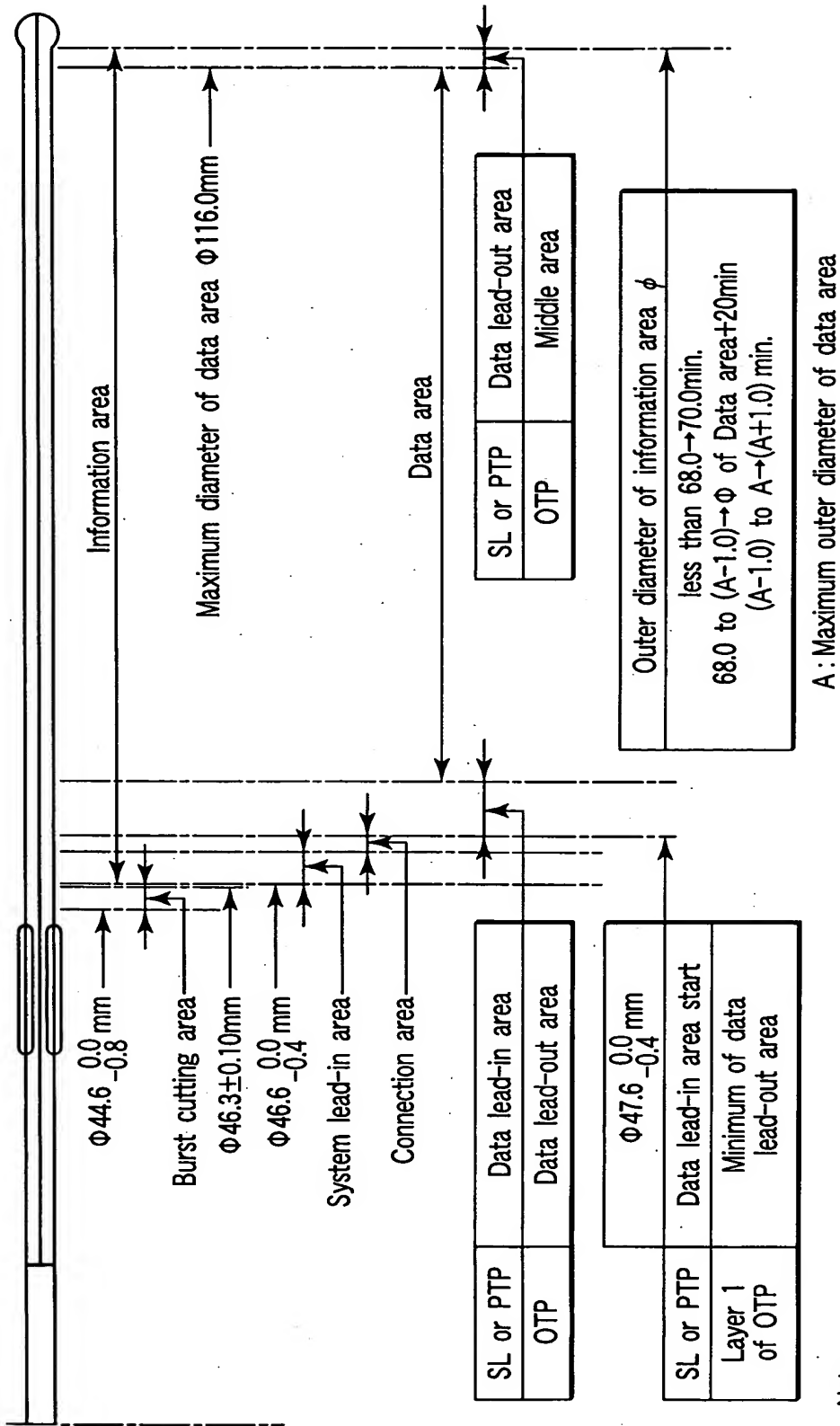


FIG. 89

Recording data density in each region in read only information recording medium

Parameter		Single layer	Dual layer
<ul style="list-style-type: none"> • User data capacity • Wavelength of laser diode • Number of openings of objective lens 		15 Gbytes/side	30 Gbytes/side
		405 nm	
		0.65	
• Data bit length	System lead-in area	0.306 μm	
	Data lead-in area	0.153 μm	
	Data area		
• Channel bit length	Data lead-out area		
	System lead-in area	0.204 μm	
	Data lead-in area	0.102 μm	
• Minimum mark length	Data area		
	Data lead-out area		
• Maximum mark length	System lead-in area	0.408 μm	
	Data lead-in area	0.204 μm	
	Data area		
• Track pitch	Data lead-out area		
	System lead-in area	2.652 μm	
	Data lead-in area	1.326 μm	
• Disk diameter	Data area		
	Data lead-out area		
	System lead-in area	0.68 μm	
• Disk thickness	Data lead-in area	0.40 μm	
	Data area		
	Data lead-out area		
<ul style="list-style-type: none"> • Cover layer thickness • Center hole diameter • Inner diameter of data area • Diameter of data area 	System lead-in area	120 mm	
	Data lead-in area	1.20 mm	
	Data area	0.6 mm	
	Data lead-out area	15.0 mm	
	System lead-in area	24.1 mm	
	Data lead-in area	58.0 mm	
<ul style="list-style-type: none"> • User data or sector • Error correction code • ECC restriction sector • Modulation 	System lead-in area	2048 bytes	
	Data lead-in area	Reed solomon multiplication code	
	Data area	RS (208, 192, 17) \times RS (182, 172, 11)	
	Data lead-out area	32 sectors	
• Correctable burst error length	System lead-in area	ETM, RLL (1, 10)	
	Data lead-in area	7.1 mm	
• Reference scan speed	Data area	6.61 m/s	
	Data lead-out area		
• Channel bit rate with reference speed	System lead-in area	32.40 Mbps	
	Data lead-in area	64.80 Mbps	
	Data area		
• User bit rate with reference speed	Data lead-out area		
	System lead-in area	18.28 Mbps	
	Data lead-in area	36.55 Mbps	
• User data or sector	Data area		
	Data lead-out area		

FIG. 90

Data lead-in area utilizing example (1)

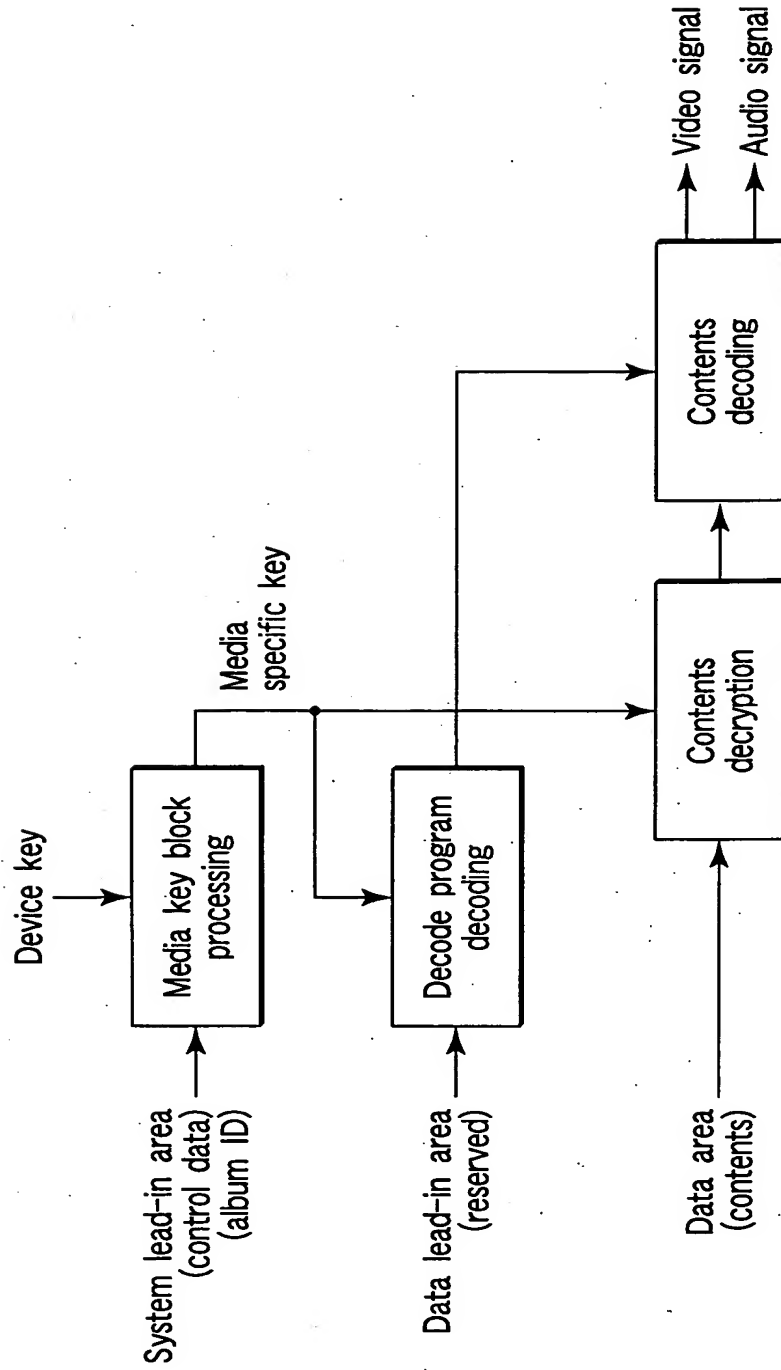
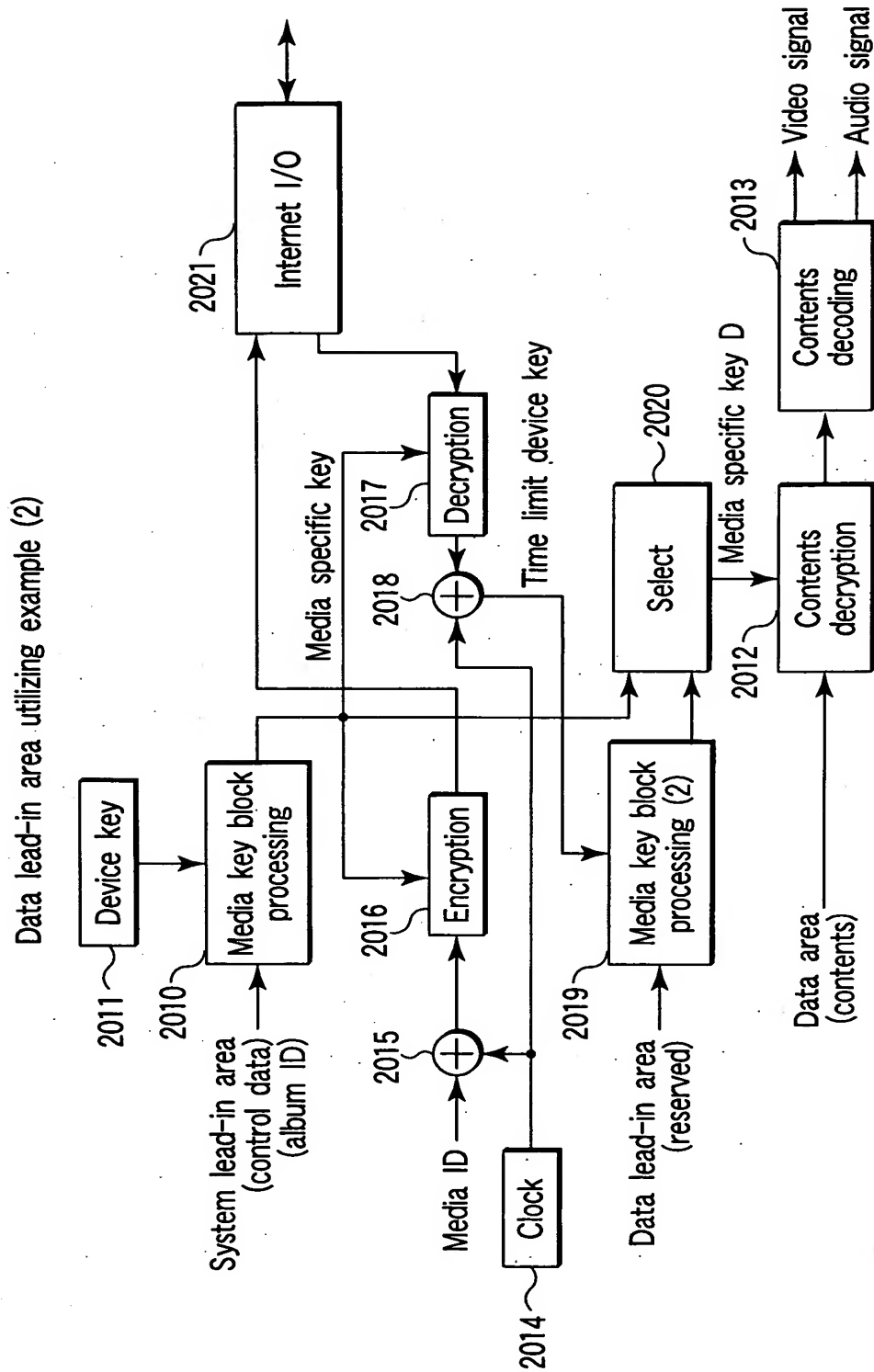


FIG. 91



Data allocation in control data zone in read only/
write once/rewritable information recording medium

Physical format information
Disk manufacturer information
Reserved

FIG. 93

Contents of information contained in physical format in
read only information recording medium

BP	Contents	Number of bytes
0	Book type and part type	1 byte
1	Disk size and maximum transfer speed of disk	1 byte
2	Disk structure	1 byte
3	Recording density	1 byte
4 to 15	Data area allocation	12 bytes
16	BCA adapter	1 byte
17 to 2047	Reserved	2031 bytes

FIG. 94

(BP 0) Book type and part type

b7	b6	b5	b4	b3	b2	b1	b0
Book type				Part type			

FIG. 95

(BP 1) Disk size and maximum transfer speed of disk

b7	b6	b5	b4	b3	b2	b1	b0
Disk size				Maximum transfer speed of disk			

FIG. 96

(BP 2) Disk structure

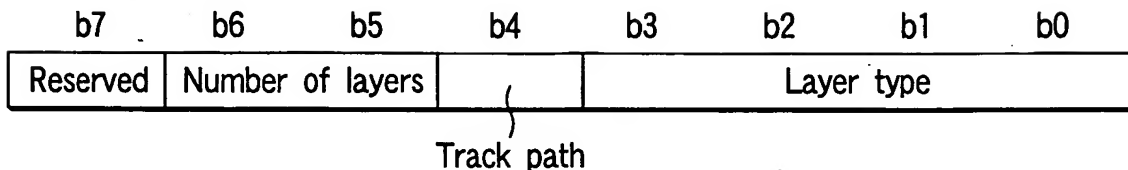


FIG. 97

(BP 3) Recording density

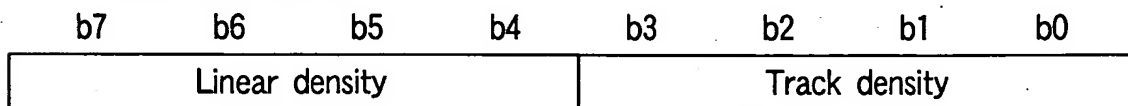


FIG. 98

Contents of data area allocation information contained in read only
/write once/rewritable information recording medium

BP	SL	PTP	OTP	Number of bytes
4	00h			1 byte
5 to 7	Number of start physical sectors in data area (03 0000h)			3 bytes
8	00h			1 byte
9 to 11	Number of end physical sectors in data area			3 bytes
12	00h			1 byte
13 to 15	00 0000h		Number of end physical sectors in layer 0	3 bytes

FIG. 99

(BP 16) BCA descriptor

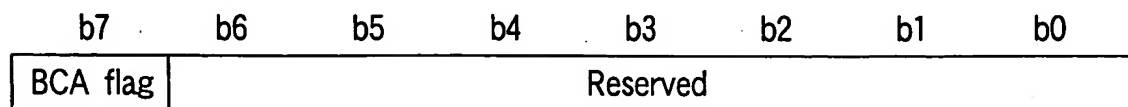


FIG. 100

Recording data density in each area in rewritable information recording medium

Parameter		Single layer
<ul style="list-style-type: none"> User data capacity Wavelength of laser diode Number of openings of objective lens 		15 Gbytes/side
		405 nm
		0.65
<ul style="list-style-type: none"> Data bit length 	System lead-in area	0.306 μm
	Data lead-in area	0.130 to 0.140 μm
	Data area	
	Data lead-out area	
<ul style="list-style-type: none"> Channel bit length 	System lead-in area	0.204 μm
	Data lead-in area	0.087 to 0.093 μm
	Data area	
	Data lead-out area	
<ul style="list-style-type: none"> Minimum mark length (2T) 	System lead-in area	0.408 μm
	Data lead-in area	0.173 to 0.187 μm
	Data area	
	Data lead-out area	
<ul style="list-style-type: none"> Maximum mark length (13T) 	System lead-in area	2.652 μm
	Data lead-in area	1.126 to 1.213 μm
	Data area	
	Data lead-out area	
<ul style="list-style-type: none"> Track pitch 	System lead-in area	0.68 μm
	Data lead-in area	0.34 μm
	Data area	
	Data lead-out area	
<ul style="list-style-type: none"> Physical address 	Data lead-in area	*WAP *WAP= Wobble Address in Periodic position
	Data area	
	Data lead-out area	
<ul style="list-style-type: none"> Disk diameter Disk thickness Center hole diameter Inner diameter of data area Diameter of data area 		120 mm 1.20 mm 15.0 mm 24.1 mm 57.89 mm
<ul style="list-style-type: none"> User data or sector Error correction code ECC restriction sector Modulation 		2048 bytes Reed solomon multiplication code RS (208, 192, 17) X RS (182, 172, 11) 32 sectors ETM, RLL (1, 10)
<ul style="list-style-type: none"> Correctable burst error length 	System lead-in area	7.1 mm
<ul style="list-style-type: none"> Reference speed 	Data lead-in area	6.0 mm
	Data area	
	Data lead-out area	
	System lead-in area	6.61 m/s
<ul style="list-style-type: none"> Channel bit rate with reference speed 	Data lead-in area	5.64 to 6.03 m/s
	Data area	
	Data lead-out area	
	System lead-in area	32.40 Mbps
<ul style="list-style-type: none"> User bit rate with reference speed 	Data lead-in area	64.80 Mbps
	Data area	
	Data lead-out area	
	System lead-in area	18.28 Mbps
<ul style="list-style-type: none"> User bit rate with reference speed 	Data lead-in area	36.55 Mbps
	Data area	
	Data lead-out area	
	System lead-in area	

FIG. 101

Data structure in lead-in area in rewritable
information recording medium

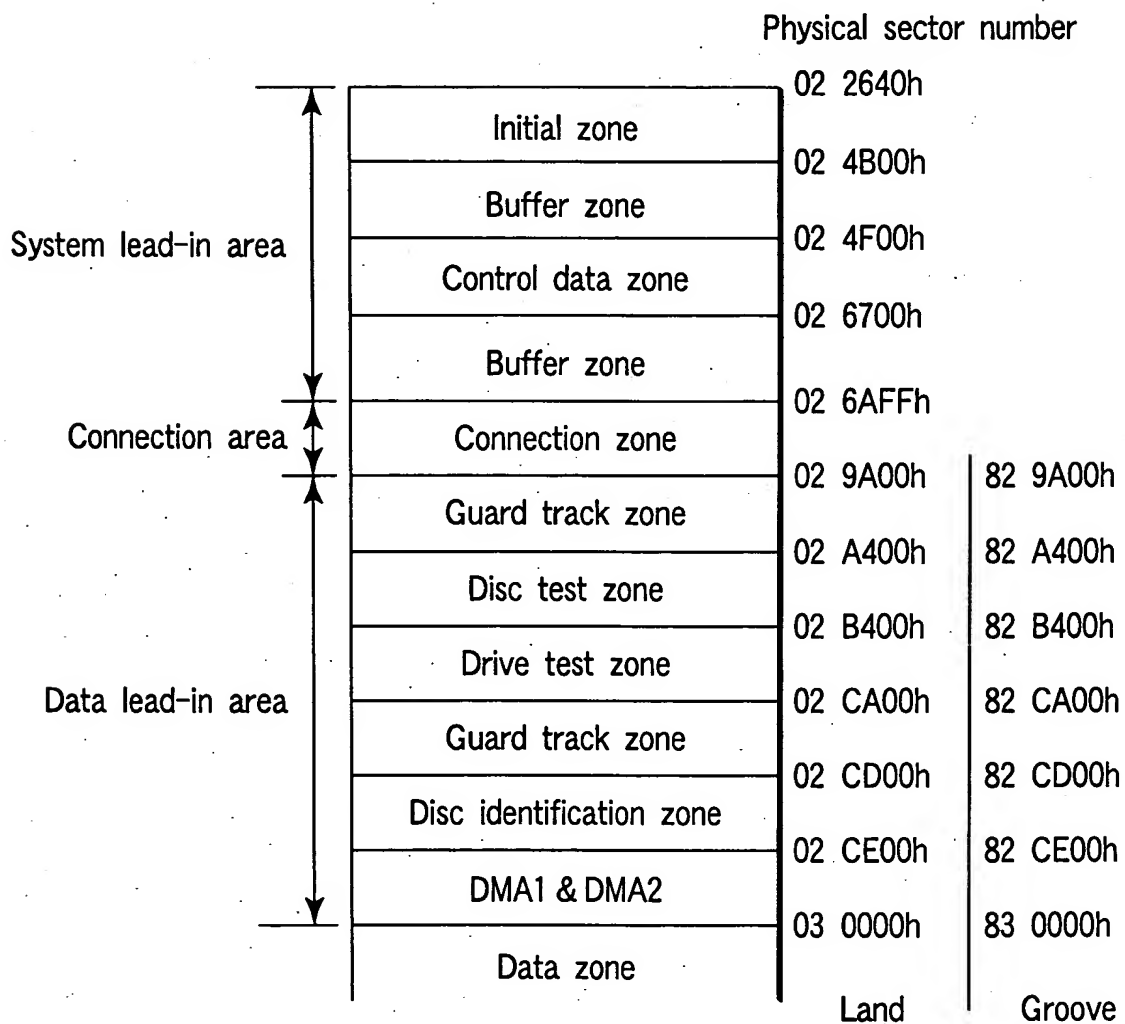


FIG. 102

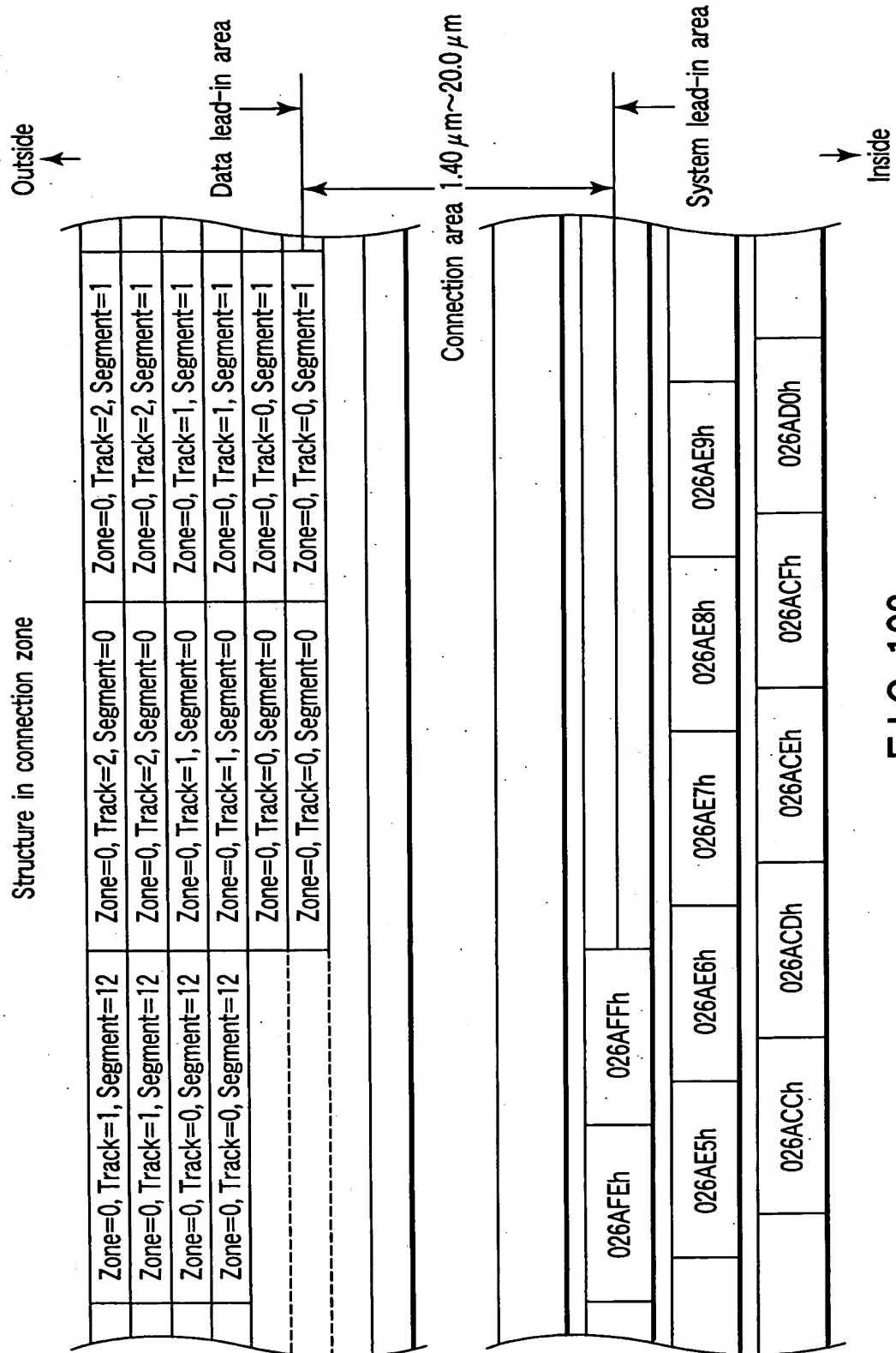


FIG. 103

Disk ID zone structure in data lead-in area

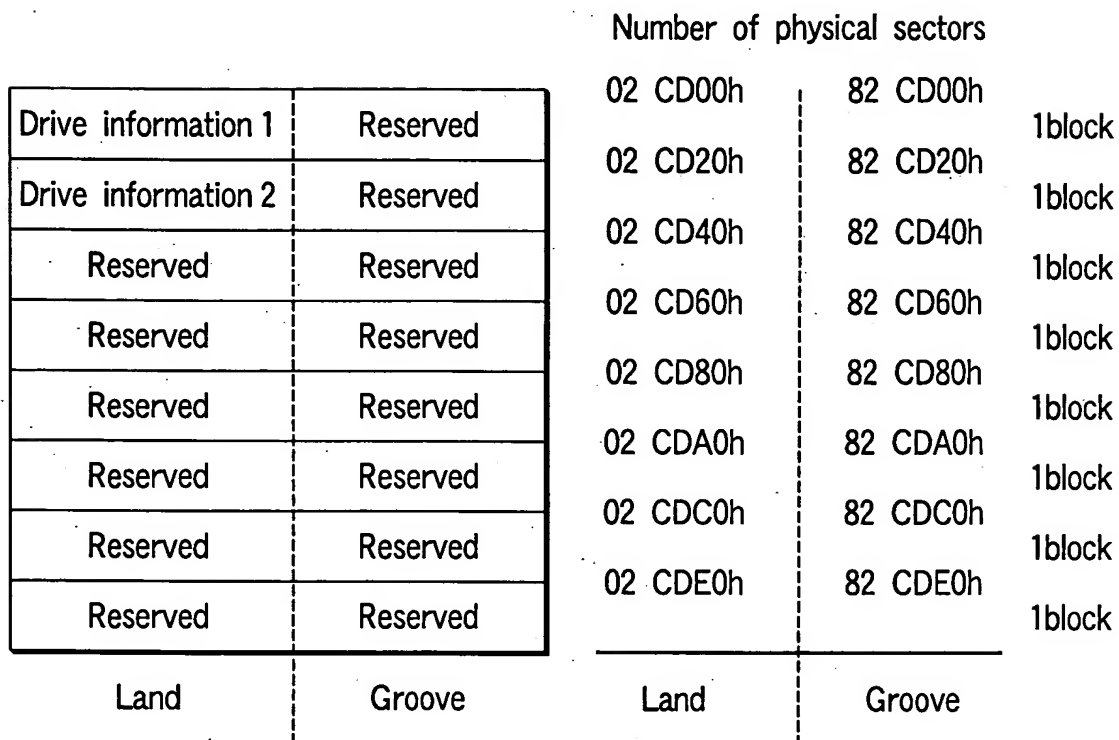


FIG. 104

Structure of drive information block

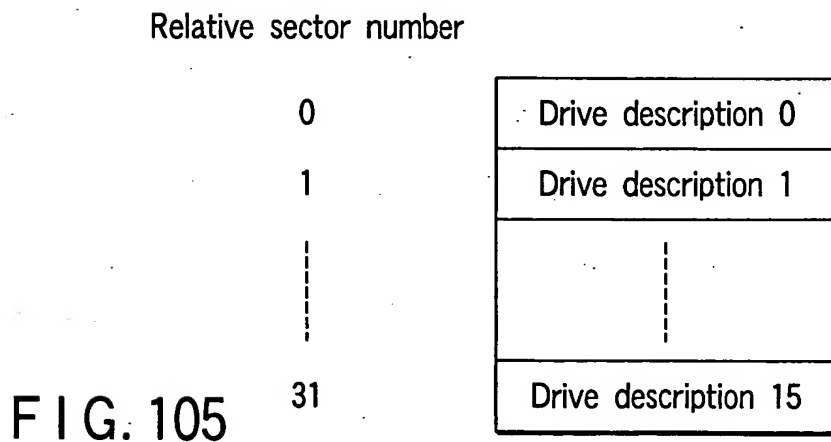


FIG. 105

Contents of drive description

BP	Contents	Number of bytes
0 to 47	Drive manufacturer's name	48 bytes
48 to 95	Additional information	48 bytes
96 to 2047	Drive state	1952 bytes

FIG. 106

Data structure in lead-out area in rewritable information
recording medium

Data area	Physical sector number	
	Land	Groove
DMA3 & DMA4	4E D740h	CE D740h
Guard track zone	4F 0940h	CF 0940h
Drive test zone	4F 0C40h	CF 0C40h
Disk test zone	4F 2240h	CF 2240h
Guard track zone	4F 3240h	CF 3240h
	Land	Groove

FIG. 107

Data layout in rewritable information recording medium

	Zone	Normal (mm)	Number of physical segments per track	Number of tracks	System or land		Groove	
					Start physical sector number (hex value)	End physical sector number (hex value)	Start physical sector number (hex value)	End physical sector number (hex value)
System lead-in area	Initial zone				022640	024AFF		
	Buffer zone				024B00	024EFF		
	Control data zone				024F00	0266FF		
	Buffer zone				026700	026AFF		
Connection area	Connection zone	23.78~23.80	---	---	---	---	---	
Data lead-in area	Guard track zone	23.80~24.10	13	5404	029A00	02A3FF	829A00	82A3FF
	Disk test zone				02A400	02B3FF	82A400	82B3FF
	Drive test zone				02B400	02C9FF	82B400	82C9FF
	Guard track zone				02CA00	02CCFF	82CA00	82CCFF
	Disk ID zone				02CD00	02CDFF	82CD00	82CDFF
	DMA1 & DMA2				02CE00	02FFFF	82CE00	82FFFF
Data area	Zone 0	24.10~25.64	13		030000	050D3F	830000	850D3F
	Zone 1	25.64~27.47	14	5390	050D40	07AEFF	850D40	87AEFF
	Zone 2	27.47~29.30	15	5390	07AF00	0A80DF	87AF00	8A80DF
	Zone 3	29.30~31.14	16	5390	0A80E0	0D82DF	8A80E0	8D82DF
	Zone 4	31.14~32.97	17	5390	0D82E0	10B4FF	8D82E0	90B4FF
	Zone 5	32.97~34.80	18	5390	10B500	14173F	90B500	94173F
	Zone 6	34.80~36.63	19	5390	141740	17A99F	941740	97A99F
	Zone 7	36.63~38.47	20	5390	17A9A0	1B6C1F	97A9A0	9B6C1F
	Zone 8	38.47~40.30	21	5390	1B6C20	1F5EBF	9B6C20	9F5EBF
	Zone 9	40.30~42.13	22	5390	1F5EC0	23817F	9F5EC0	A3817F
	Zone 10	42.13~43.97	23	5390	238180	27D45F	A38180	A7D45F
	Zone 11	43.97~45.80	24	5390	27D460	2C575F	A7D460	AC575F
	Zone 12	45.80~47.63	25	5390	2C5760	310A7F	AC5760	B10A7F
	Zone 13	47.63~49.46	26	5390	310A80	35EDBF	B10A80	B5EDBF
	Zone 14	49.46~51.30	27	5390	35EDC0	3B011F	B5EDC0	BB011F
	Zone 15	51.30~53.13	28	5390	3B0120	40449F	BB0120	C0449F
	Zone 16	53.13~54.96	29	5390	4044A0	45B83F	C044A0	C5B83F
	Zone 17	54.96~56.79	30	5390	45B840	4B5BFF	C5B840	CB5BFF
	Zone 18	56.79~57.89	31	3220	4B5C00	4ED73F	CB5C00	CED73F
Data lead-in area	DM3 & DMA4	57.89~58.6	31	1792	4ED740	4F093F	CED740	CF093F
	Guard track zone				4F0940	4F0C3F	CF0940	CF0C3F
	Drive test zone				4F0C40	4F223F	CF0C40	CF223F
	Disk test zone				4F2240	4F323F	CF2240	CF323F
	Guard track zone				4F3240	50C73F	CF3240	D0C73F

FIG. 108

Address number setting method in data area in rewritable information recording medium

L/G	Zone	Number of ECC blocks	Start physical sector number	Guard area		Groove				End physical sector number	Start LSN of zone
				Physical sector number	Physical sector number	Physical sector number	Physical sector number	Physical sector number	Physical sector number		
L	0	4202	30000								
L	1	5390	50040	50040	50040	50040	50040	50040	50040	50040	ED00
L	2	5775	7AF00	7AF00	7AF00	7AF00	7AF00	7AF00	7AF00	7AF00	ED00
L	3	6160	8A0E0	8A0E0	8A0E0	8A0E0	8A0E0	8A0E0	8A0E0	8A0E0	ED00
L	4	6545	D82E0	D82E0	D82E0	D82E0	D82E0	D82E0	D82E0	D82E0	ED00
L	5	6930	10E500	10E500	10E500	10E500	10E500	10E500	10E500	10E500	ED00
L	6	7315	141740	141740	141740	141740	141740	141740	141740	141740	ED00
L	7	7700	17A940	17A940	17A940	17A940	17A940	17A940	17A940	17A940	ED00
L	8	8085	1B6C20	1B6C20	1B6C20	1B6C20	1B6C20	1B6C20	1B6C20	1B6C20	ED00
L	9	8470	1F5EC0	1F5EC0	1F5EC0	1F5EC0	1F5EC0	1F5EC0	1F5EC0	1F5EC0	ED00
L	10	8855	238180	238180	238180	238180	238180	238180	238180	238180	ED00
L	11	9240	27D460	27D460	27D460	27D460	27D460	27D460	27D460	27D460	ED00
L	12	9625	2C5760	2C5760	2C5760	2C5760	2C5760	2C5760	2C5760	2C5760	ED00
L	13	10010	310A80	310A80	310A80	310A80	310A80	310A80	310A80	310A80	ED00
L	14	10395	35EDC0	35EDC0	35EDC0	35EDC0	35EDC0	35EDC0	35EDC0	35EDC0	ED00
L	15	10780	3B0120	3B0120	3B0120	3B0120	3B0120	3B0120	3B0120	3B0120	ED00
L	16	11165	4044A0	4044A0	4044A0	4044A0	4044A0	4044A0	4044A0	4044A0	ED00
L	17	11550	458840	458840	458840	458840	458840	458840	458840	458840	ED00
L	18	7130	485C00	485C00	485C00	485C00	485C00	485C00	485C00	485C00	ED00
G	0	4202	830000								
G	1	5390	850D40	850D40	850D40	850D40	850D40	850D40	850D40	850D40	ED00
G	2	5775	87AF00	87AF00	87AF00	87AF00	87AF00	87AF00	87AF00	87AF00	ED00
G	3	6160	8A80E0	8A80E0	8A80E0	8A80E0	8A80E0	8A80E0	8A80E0	8A80E0	ED00
G	4	6545	8D82E0	8D82E0	8D82E0	8D82E0	8D82E0	8D82E0	8D82E0	8D82E0	ED00
G	5	6930	908500	908500	908500	908500	908500	908500	908500	908500	ED00
G	6	7315	941740	941740	941740	941740	941740	941740	941740	941740	ED00
G	7	7700	97A940	97A940	97A940	97A940	97A940	97A940	97A940	97A940	ED00
G	8	8085	9B6C20	9B6C20	9B6C20	9B6C20	9B6C20	9B6C20	9B6C20	9B6C20	ED00
G	9	8470	9F5EC0	9F5EC0	9F5EC0	9F5EC0	9F5EC0	9F5EC0	9F5EC0	9F5EC0	ED00
G	10	8855	A38180	A38180	A38180	A38180	A38180	A38180	A38180	A38180	ED00
G	11	9240	ATD460	ATD460	ATD460	ATD460	ATD460	ATD460	ATD460	ATD460	ED00
G	12	9625	AC5760	AC5760	AC5760	AC5760	AC5760	AC5760	AC5760	AC5760	ED00
G	13	10010	B10A80	B10A80	B10A80	B10A80	B10A80	B10A80	B10A80	B10A80	ED00
G	14	10395	B5EDC0	B5EDC0	B5EDC0	B5EDC0	B5EDC0	B5EDC0	B5EDC0	B5EDC0	ED00
G	15	10780	B80120	B80120	B80120	B80120	B80120	B80120	B80120	B80120	ED00
G	16	11165	C044A0	C044A0	C044A0	C044A0	C044A0	C044A0	C044A0	C044A0	ED00
G	17	11550	C58840	C58840	C58840	C58840	C58840	C58840	C58840	C58840	ED00
G	18	7130	C85C00	C85C00	C85C00	C85C00	C85C00	C85C00	C85C00	C85C00	ED00
Total											

Data structure in lead-in area of write once information recording medium

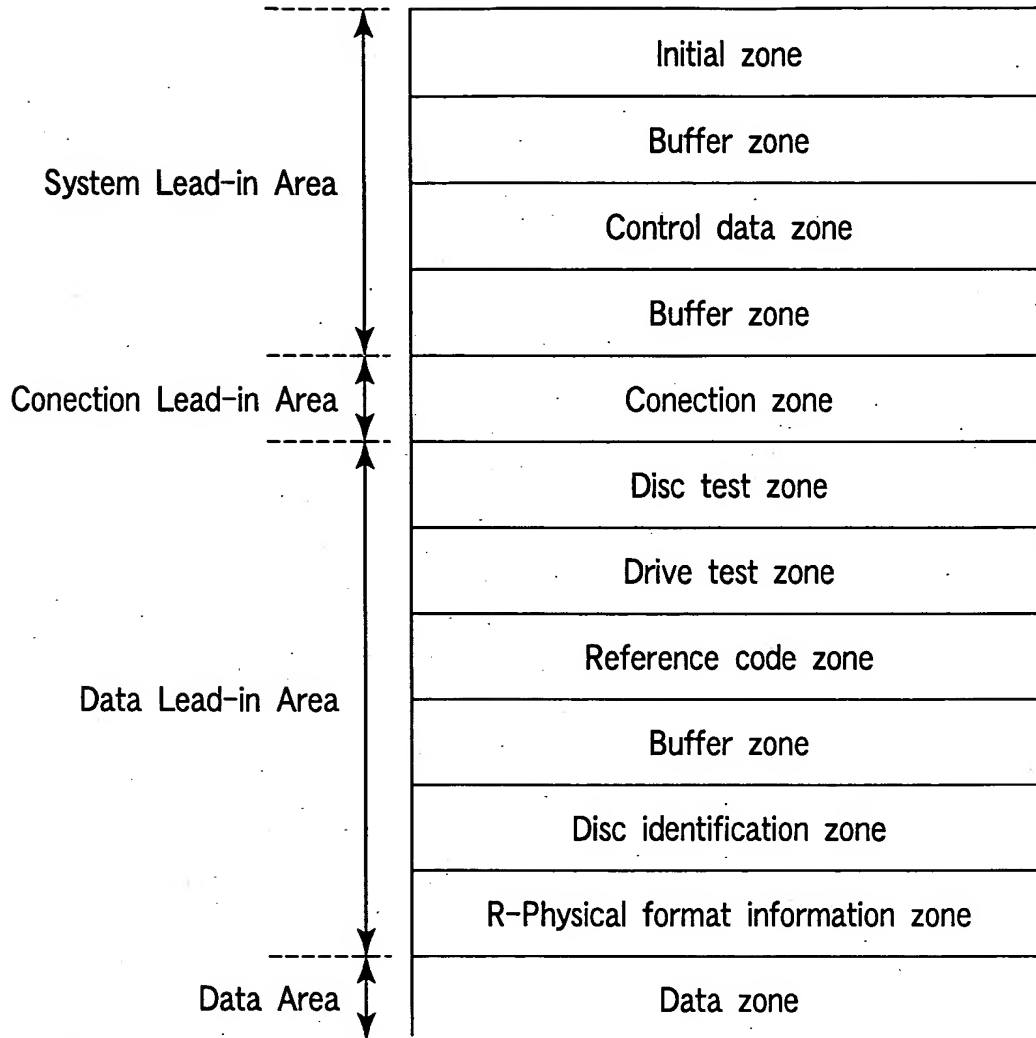


FIG. 110

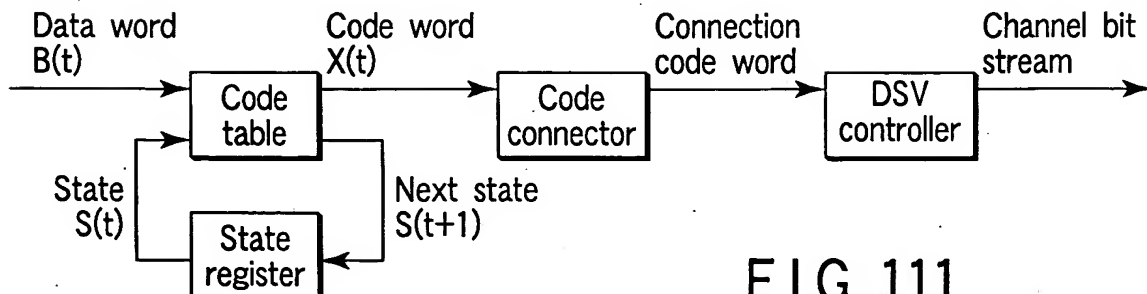


FIG. 111

Concatenation rule

Index	Preceding code word	Current code word	Concatenated code work
1	??0101 010101	010??? ??????	??0100 000000 010??? ??????
2	??0101 010101	001??? ??????	??0100 000000 001??? ??????
3	??1001 010101	010??? ??????	??1000 000000 010??? ??????
4	?????0 101010	101010 ??????	?????0 100000 000010 ??????
5	?????1 001010	101010 ??????	?????1 000000 000010 ??????
6	?????? ?0101	010101 010???	?????? ?0100 000000 010???
7	?????? ?0101	010101 001???	?????? ?0100 000000 001???
8	?????? ?1001	010101 010???	?????? ?1000 000000 010???
9	?????? ?????1	001010 101010	?????? ?????1 000000 000010

FIG. 112

Concatenation between code word and sync code

Index	Preceding code word	Succeeding sync code	Concatenated code
S	?????0 00000#	SY3	?????0 000001+SY3

FIG. 113

Separation rule

Index	Readout code word	Current code word	Succeeding code word
1	?????? ?00000 0000?? ??????	?????? ?01010	1010?? ??????
2	?????? ?????00 000000 0?????	?????? ?????01	010101 0?????
3	?????? ??????? 000000 0000??	?????? ???????	001010 1010??

FIG. 114

Conversion table in modulation system

Data word	State 0		State 1		State 2	
	Code word	Next state	Code word	Next state	Code word	Next state
00	100010 00000*	0	010100 01000*	0	010100 01000*	0
01	100010 00000#	1	010100 010001	1	010100 010001	1
02	100010 000010	0	010100 010010	0	010100 010010	0
03	100010 000010	1	010100 010010	1	010100 010010	1
04	100010 10000*	0	010100 01010*	0	010100 01010*	0
05	100010 10000#	1	010100 010101	1	010100 010101	1
06	100010 100010	0	010100 010100	2	010100 010100	2
07	100010 100010	1	010100 010000	2	010100 010000	2
08	100010 10100*	0	010100 00#00*	0	010100 00#00*	0
09	100010 101001	1	010100 00#001	1	010100 00#001	1
0A	100010 101010	0	010100 00#010	0	010100 00#010	0
0B	100010 101010	1	010100 00#010	1	010100 00#010	1
0C	100010 10010*	0	010100 00010*	0	010100 00010*	0
0D	100010 100101	1	010100 000101	1	010100 000101	1
0E	100010 100100	2	010100 000100	2	010100 000100	2
0F	100010 101000	2	010100 001000	2	010100 001000	2
10	100010 01000*	0	010000 01000*	0	010000 01000*	0
11	100010 010001	1	010000 010001	1	010000 010001	1
12	100010 010010	0	010000 010010	0	010000 010010	0
13	100010 010010	1	010000 010010	1	010000 010010	1
14	100010 01010*	0	010000 01010*	0	010000 01010*	0
15	100010 010101	1	010000 010101	1	010000 010101	1
16	100010 010100	2	010000 010100	2	010000 010100	2
17	100010 010000	2	010000 010000	2	010000 010000	2
18	100010 00100*	0	010000 00100*	0	010000 00100*	0
19	100010 001001	1	010000 001001	1	010000 001001	1
1A	100010 001010	0	010000 00#010	0	010000 00#010	0
1B	100010 001010	1	010000 00#010	1	010000 00#010	1
1C	100010 00010*	0	010000 00010*	0	010000 00010*	0
1D	100010 000101	1	010000 000101	1	010000 000101	1
1E	100010 000100	2	010000 000100	2	010000 000100	2
1F	100010 001000	2	010000 001000	2	010000 001000	2
20	100001 00000*	0	010101 00000*	0	010101 00000*	0
21	100001 00000#	1	010101 00000#	1	010101 00000#	1
22	100001 000010	0	010101 000010	0	010101 000010	0
23	100001 000010	1	010101 000010	1	010101 000010	1
24	100000 10000*	0	010100 10000*	0	010100 10000*	0
25	100000 10000#	1	010100 10000#	1	010100 10000#	1
26	100000 100010	0	010100 100010	0	010100 100010	0
27	100000 100010	1	010100 100010	1	010100 100010	1
28	100000 10100*	0	010100 10100*	0	010100 10100*	0
29	100000 101001	1	010100 101001	1	010100 101001	1
2A	100000 101010	0	010100 101010	0	010100 101010	0
2B	100000 101010	1	010100 101010	1	010100 101010	1
2C	100000 10010*	0	010100 10010*	0	010100 10010*	0
2D	100000 100101	1	010100 100101	1	010100 100101	1
2E	100000 100100	2	010100 100100	2	010100 100100	2
2F	100000 101000	2	010100 101000	2	010100 101000	2

FIG. 115

Data word	State 0		State 1		State 2	
	Code word	Next state	Code word	Next state	Code word	Next state
30	10000# 01000*	0	010101 01000*	0	010101 01000*	0
31	10000# 010001	1	010101 010001	1	010101 010001	1
32	10000# 010010	0	010101 010010	0	010101 010010	0
33	10000# 010010	1	010101 010010	1	010101 010010	1
34	10000# 01010*	0	010000 00000*	0	010000 00000*	0
35	100000 010101	1	010000 000001	1	010000 000001	1
36	10000# 010100	2	010101 010100	2	010101 010100	2
37	10000# 010000	2	010101 010000	2	010101 010000	2
38	10000# 00100*	0	010101 00100*	0	010101 00100*	0
39	10000# 001001	1	010101 001001	1	010101 001001	1
3A	10000# 001010	0	010101 001010	0	010101 001010	0
3B	10000# 001010	1	010101 001010	1	010101 001010	1
3C	10000# 00010*	0	010101 00010*	0	010101 00010*	0
3D	10000# 000101	1	010101 000101	1	010101 000101	1
3E	10000# 000100	2	010101 000100	2	010101 000100	2
3F	10000# 001000	2	010101 001000	2	010101 001000	2
40	101010 00000*	0	010010 00000*	0	010010 00000*	0
41	101010 00000#	1	010010 00000#	1	010010 00000#	1
42	101010 000010	0	010010 000010	0	010010 000010	0
43	101010 000010	1	010010 000010	1	010010 000010	1
44	101010 10000*	0	010010 10000*	0	010010 10000*	0
45	101010 10000#	1	010010 10000#	1	010010 10000#	1
46	101010 100010	0	010010 100010	0	010010 100010	0
47	101010 100010	1	010010 100010	1	010010 100010	1
48	000000 00100*	0	010010 10100*	0	010010 10100*	0
49	100000 000001	1	010010 101001	1	010010 101001	1
4A	100000 000010	0	010010 101010	0	010010 101010	0
4B	100000 000010	1	010010 101010	1	010010 101010	1
4C	101010 10010*	0	010010 10010*	0	010010 10010*	0
4D	101010 100101	1	010010 100101	1	010010 100101	1
4E	101010 100100	2	010010 100100	2	010010 100100	2
4F	000000 001000	2	010010 101000	2	010010 101000	2
50	101010 01000*	0	010010 01000*	0	010010 01000*	0
51	101010 010001	1	010010 010001	1	010010 010001	1
52	101010 010010	0	010010 010010	0	010010 010010	0
53	101010 010010	1	010010 010010	1	010010 010010	1
54	101010 01010*	0	010010 01010*	0	010010 01010*	0
55	101010 010101	1	010010 010101	1	010010 010101	1
56	101010 010100	2	010010 010100	2	010010 010100	2
57	101010 010000	2	010010 010000	2	010010 010000	2
58	101010 00100*	0	010010 00100*	0	010010 00100*	0
59	101010 001001	1	010010 001001	1	010010 001001	1
5A	101010 001010	0	010010 001010	0	010010 001010	0
5B	101010 001010	1	010010 001010	1	010010 001010	1
5C	101010 00010*	0	010010 00010*	0	010010 00010*	0
5D	101010 000101	1	010010 000101	1	010010 000101	1
5E	101010 000100	2	010010 000100	2	010010 000100	2
5F	101010 001000	2	010010 001000	2	010010 001000	2

FIG. 116

Data word	State 0		State 1		State 2	
	Code word	Next state	Code word	Next state	Code word	Next state
60	101001 00000*	0	010001 00000*	0	010001 00000*	0
61	101001 00000#	1	010001 000001	1	010001 000001	1
62	101001 000010	0	010001 000010	0	010001 000010	0
63	101001 000010	1	010001 000010	1	010001 000010	1
64	101000 10000*	0	010000 10000*	0	010000 10000*	0
65	101000 10000#	1	010000 10000#	1	010000 10000#	1
66	101000 100010	0	010000 100010	0	010000 100010	0
67	101000 100010	1	010000 100010	1	010000 100010	1
68	101000 10100*	0	010000 10100*	0	010000 10100*	0
69	101000 101001	1	010000 101001	1	010000 101001	1
6A	101000 101010	0	010000 101010	0	010000 101010	0
6B	101000 101010	1	010000 101010	1	010000 101010	1
6C	101000 10010*	0	010000 10010*	0	010000 10010*	0
6D	101000 100101	1	010000 100101	1	010000 100101	1
6E	101000 100100	2	010000 100100	2	010000 100100	2
6F	101000 101000	2	010000 101000	2	010000 101000	2
70	101001 01000*	0	010001 01000*	0	010001 01000*	0
71	101001 010001	1	010001 010001	1	010001 010001	1
72	101001 010010	0	010001 010010	0	010001 010010	0
73	101001 010010	1	010001 010010	1	010001 010010	1
74	101001 01010*	0	010001 01010*	0	010001 01010*	0
75	101001 010101	1	010001 000000	1	010001 000000	1
76	101001 010100	2	010001 010100	2	010001 010100	2
77	101001 010000	2	010001 010000	2	010001 010000	2
78	101001 00100*	0	010001 00100*	0	010001 00100*	0
79	101001 001001	1	010001 001001	1	010001 001001	1
7A	101001 001010	0	010001 001010	0	010001 001010	0
7B	101001 001010	1	010001 001010	1	010001 001010	1
7C	101001 00010*	0	010001 00010*	0	010001 00010*	0
7D	101001 000101	1	010001 000101	1	010001 000101	1
7E	101001 000100	2	010001 000100	2	010001 000100	2
7F	101001 001000	2	010001 001000	2	010001 001000	2
80	100100 01000*	0	000100 01000*	0	000100 01000*	0
81	100100 010001	1	000100 010001	1	000100 010001	1
82	100100 010010	0	000100 010010	0	000100 010010	0
83	100100 010010	1	000100 010010	1	000100 010010	1
84	100100 01010*	0	000100 01010*	0	000100 01010*	0
85	100100 010101	1	000100 010101	1	000100 010101	1
86	100100 010100	2	000100 010100	2	000100 010100	2
87	100100 010000	2	000100 010000	2	000100 010000	2
88	100100 00#00*	0	000100 00#00*	0	000100 00#00*	0
89	100100 00#001	1	000100 00#001	1	000100 00#001	1
8A	100100 00#010	0	000100 00#010	0	000100 00#010	0
8B	100100 00#010	1	000100 00#010	1	000100 00#010	1
8C	100100 00010*	0	000100 00010*	0	000100 00010*	0
8D	100100 000101	1	000100 000101	1	000100 000101	1
8E	100100 000100	2	000100 000100	2	000100 000100	2
8F	100100 001000	2	000100 001000	2	000100 001000	2

FIG. 117

Data word	State 0		State 1		State 2	
	Code word	Next state	Code word	Next state	Code word	Next state
90	101000 01000*	0	001000 01000*	0	001000 01000*	0
91	101000 010001	1	001000 010001	1	001000 010001	1
92	101000 010010	0	001000 010010	0	001000 010010	0
93	101000 010010	1	001000 010010	1	001000 010010	1
94	101000 01010*	0	001000 01010*	0	001000 01010*	0
95	101000 010101	1	001000 010101	1	001000 010101	1
96	101000 010100	2	001000 010100	2	001000 010100	2
97	101000 010000	2	001000 010000	2	001000 010000	2
98	101000 00#00*	0	001000 00#00*	0	001000 00#00*	0
99	101000 00#001	1	001000 00#001	1	001000 00#001	1
9A	101000 00#010	0	001000 00#010	0	001000 00#010	0
9B	101000 00#010	1	001000 00#010	1	001000 00#010	1
9C	101000 00010*	0	001000 00010*	0	001000 00010*	0
9D	101000 000101	1	001000 000101	1	001000 000101	1
9E	101000 000100	2	001000 000100	2	001000 000100	2
9F	101000 001000	2	001000 001000	2	001000 001000	2
A0	100101 00000*	0	000101 00000*	0	000101 00000*	0
A1	100101 00000#	1	000101 00000#	1	000101 00000#	1
A2	100101 000010	0	000101 000010	0	000101 000010	0
A3	100101 000010	1	000101 000010	1	000101 000010	1
A4	100100 10000*	0	000100 10000*	0	000100 10000*	0
A5	100100 10000#	1	000100 10000#	1	000100 10000#	1
A6	100100 100010	0	000100 100010	0	000100 100010	0
A7	100100 100010	1	000100 100010	1	000100 100010	1
A8	100100 10100*	0	000100 10100*	0	000100 10100*	0
A9	100100 101001	1	000100 101001	1	000100 101001	1
AA	100100 101010	0	000100 101010	0	000100 101010	0
AB	100100 101010	1	000100 101010	1	000100 101010	1
AC	100100 10010*	0	000100 10010*	0	000100 10010*	0
AD	100100 100101	1	000100 100101	1	000100 100101	1
AE	100100 100100	2	000100 100100	2	000100 100100	2
AF	100100 101000	2	000100 101000	2	000100 101000	2
B0	100101 01000*	0	000101 01000*	0	000101 01000*	0
B1	100101 010001	1	000101 010001	1	000101 010001	1
B2	100101 010010	0	000101 010010	0	000101 010010	0
B3	100101 010010	1	000101 010010	1	000101 010010	1
B4	100101 01010*	0	000101 01010*	0	000101 01010*	0
B5	100101 010101	1	000101 010101	1	000101 010101	1
B6	100101 010100	2	000101 010100	2	000101 010100	2
B7	100101 010000	2	000101 010000	2	000101 010000	2
B8	100101 00100*	0	000101 00100*	0	000101 00100*	0
B9	100101 001001	1	000101 001001	1	000101 001001	1
BA	100101 001010	0	000101 001010	0	000101 001010	0
BB	100101 001010	1	000101 001010	1	000101 001010	1
BC	100101 00010*	0	000101 00010*	0	000101 00010*	0
BD	100101 000101	1	000101 000101	1	000101 000101	1
BE	100101 000100	2	000101 000100	2	000101 000100	2
BF	100101 001000	2	000101 001000	2	000101 001000	2

FIG. 118

Data word	State 0		State 1		State 2	
	Code word	Next state	Code word	Next state	Code word	Next state
C0	000010 00000*	0	001010 00000*	0	00#010 00000*	0
C1	000010 00000#	1	001010 00000#	1	00#010 00000#	1
C2	000010 000010	0	001010 000010	0	00#010 000010	0
C3	000010 000010	1	001010 000010	1	00#010 000010	1
C4	000010 10000*	0	001010 10000*	0	00#010 10000*	0
C5	000010 10000#	1	001010 10000#	1	00#010 10000#	1
C6	000010 100010	0	001010 100010	0	00#010 100010	0
C7	000010 100010	1	001010 100010	1	00#010 100010	1
C8	000010 10100*	0	001010 10100*	0	00#010 10100*	0
C9	000010 101001	1	001010 101001	1	00#010 101001	1
CA	000010 101010	0	001000 000010	0	001000 000010	0
CB	000010 101010	1	001010 101010	1	00#010 101010	1
CC	000010 10010*	0	001010 10010*	0	00#010 10010*	0
CD	000010 100101	1	001010 100101	1	00#010 100101	1
CE	000010 100100	2	001010 100100	2	00#010 100100	2
CF	000010 101000	2	001010 101000	2	00#010 101000	2
D0	000010 01000*	0	001010 01000*	0	00#010 01000*	0
D1	000010 010001	1	001010 010001	1	00#010 010001	1
D2	000010 010010	0	001010 010010	0	00#010 010010	0
D3	000010 010010	1	001010 010010	1	00#010 010010	1
D4	000010 01010*	0	001010 01010*	0	00#010 01010*	0
D5	000010 010101	1	001010 010101	1	00#010 010101	1
D6	000010 010100	2	001010 010100	2	00#010 010100	2
D7	000010 010000	2	001010 010000	2	00#010 010000	2
D8	000010 00100*	0	001010 00100*	0	00#010 00100*	0
D9	000010 001001	1	001010 001001	1	00#010 001001	1
DA	000010 001010	0	001010 001010	0	00#010 001010	0
DB	000010 001010	1	001010 001010	1	00#010 001010	1
DC	000010 00010*	0	001010 00010*	0	00#010 00010*	0
DD	000010 000101	1	001010 000101	1	00#010 000101	1
DE	000010 000100	2	001010 000100	2	00#010 000100	2
DF	000010 001000	2	001010 001000	2	00#010 001000	2
E0	000001 00000*	0	001001 00000*	0	00#001 00000*	0
E1	000001 00000#	1	001001 00000#	1	00#001 00000#	1
E2	000001 000010	0	001001 000010	0	00#001 000010	0
E3	000001 000010	1	001001 000010	1	00#001 000010	1
E4	000000 10000*	0	001000 10000*	0	00#000 10000*	0
E5	000000 10000#	1	001000 10000#	1	00#000 10000#	1
E6	000000 100010	0	001000 100010	0	00#000 100010	0
E7	000000 100010	1	001000 100010	1	00#000 100010	1
E8	000000 10100*	0	001000 10100*	0	00#000 10100*	0
E9	000000 101001	1	001000 101001	1	00#000 101001	1
EA	000000 101010	0	001000 101010	0	00#000 101010	0
EB	000000 101010	1	001000 101010	1	00#000 101010	1
EC	000000 10010*	0	001000 10010*	0	00#000 10010*	0
ED	000000 100101	1	001000 100101	1	00#000 100101	1
EE	000000 100100	2	001000 100100	2	00#000 100100	2
EF	000000 101000	2	001000 101000	2	00#000 101000	2

FIG. 119

Data word	State 0		State 1		State 2	
	Code word	Next state	Code word	Next state	Code word	Next state
F0	00000# 01000*	0	001001 01000*	0	00#001 01000*	0
F1	00000# 010001	1	001001 010001	1	00#001 010001	1
F2	00000# 010010	0	001001 010010	0	00#001 010010	0
F3	00000# 010010	1	001001 010010	1	00#001 010010	1
F4	00000# 01010*	0	001001 01010*	0	00#001 01010*	0
F5	000000 010101	1	001001 010101	1	001001 010101	1
F6	00000# 010100	2	001001 010100	2	00#001 010100	2
F7	00000# 010000	2	001001 010000	2	00#001 010000	2
F8	000001 00100*	0	001001 00100*	0	00#001 00100*	0
F9	00000# 001001	1	001001 001001	1	00#001 001001	1
FA	00000# 001010	0	001001 001010	0	00#001 001010	0
FB	00000# 001010	1	001001 001010	1	00#001 001010	1
FC	00000# 00010*	0	001001 00010*	0	00#001 00010*	0
FD	00000# 000101	1	001001 000101	1	00#001 000101	1
FE	00000# 000100	2	001001 000100	2	00#001 000100	2
FF	000001 001000	2	001001 001000	2	00#001 001000	2

FIG. 120

Demodulation table in modulation system

Current code word	Data word		
	Case 1	Case 2	Case 3
000000 000100	FC	FE	FE
000000 000101	Z	FC	FD
000000 001000	48	4F	4F
000000 001001	Z	48	F9
000000 001010	FA	FA	FB
000000 010000	F0	F7	F7
000000 010001	Z	F0	F1
000000 010010	F2	F2	F3
000000 010100	F4	F6	F6
000000 010101	Z	F4	F5
000000 100000	E4	Z	E5
000000 100001	Z	E4	E5
000000 100010	E6	E6	E7
000000 100100	EC	EE	EE
000000 100101	Z	EC	ED
000000 101000	E8	EF	EF
000000 101001	Z	E8	E9
000000 101010	EA	EA	EB
000001 000000	E0	Z	E1
000001 000001	Z	E0	E1
000001 000010	E2	E2	E3
000001 000100	FC	FE	FE
000001 000101	Z	FC	FD
000001 001000	F8	FF	FF
000001 001001	Z	F8	F9
000001 001010	FA	FA	FB
000001 010000	F0	F7	F7
000001 010001	Z	F0	F1
000001 010010	F2	F2	F3
000001 010100	F4	F6	F6
000001 010101	Z	F4	Z
000010 000000	C0	Z	C1
000010 000001	Z	C0	C1
000010 000010	C2	C2	C3
000010 000100	DC	DE	DE
000010 000101	Z	DC	DD
000010 001000	D8	DF	DF
000010 001001	Z	D8	D9

FIG. 121

Current code word	Data word		
	Case 1	Case 2	Case 3
000010 001010	DA	DA	DB
000010 010000	D0	D7	D7
000010 010001	Z	D0	D1
000010 010010	D2	D2	D3
000010 010100	D4	D6	D6
000010 010101	Z	D4	D5
000010 100000	C4	Z	C5
000010 100001	Z	C4	C5
000010 100010	C6	C6	C7
000010 100100	CC	CE	CE
000010 100101	Z	CC	CD
000010 101000	C8	CF	CF
000010 101001	Z	C8	C9
000010 101010	CA	CA	CB
000100 000000	88	Z	B5
000100 000001	Z	88	89
000100 000010	8A	8A	8B
000100 000100	8C	8E	8E
000100 000101	Z	8C	8D
000100 001000	88	8F	8F
000100 001001	Z	88	89
000100 001010	8A	8A	8B
000100 010000	80	87	87
000100 010001	Z	80	81
000100 010010	82	82	83
000100 010100	84	86	86
000100 010101	Z	84	85
000100 100000	A4	Z	A5
000100 100001	Z	A4	A5
000100 100010	A6	A6	A7
000100 100100	AC	AE	AE
000100 100101	Z	AC	AD
000100 101000	A8	AF	AF
000100 101001	Z	A8	A9
000100 101010	AA	AA	AB
000101 000000	A0	Z	A1
000101 000001	Z	A0	A1
000101 000010	A2	A2	A3

FIG. 122

Current code word	Data word		
	Case 1	Case 2	Case 3
000101 000100	BC	BE	BE
000101 000101	Z	BC	BD
000101 001000	B8	BF	BF
000101 001001	Z	B8	B9
000101 001010	BA	BA	BB
000101 010000	B0	B7	B7
000101 010001	Z	B0	B1
000101 010010	B2	B2	B3
000101 010100	B4	B6	B6
000101 010101	Z	B4	B5
001000 000000	98	Z	F5
001000 000001	Z	98	99
001000 000010	CA	CA	9B
001000 000100	9C	9E	9E
001000 000101	Z	9C	9D
001000 001000	98	9F	9F
001000 001001	Z	98	99
001000 001010	9A	9A	9B
001000 010000	90	97	97
001000 010001	Z	90	91
001000 010010	92	92	93
001000 010100	94	96	96
001000 010101	Z	94	95
001000 100000	E4	Z	E5
001000 100001	Z	E4	E5
001000 100010	E6	E6	E7
001000 100100	EC	EE	EE
001000 100101	Z	EC	ED
001000 101000	E8	EF	EF
001000 101001	Z	E8	E9
001000 101010	EA	EA	EB
001001 000000	E0	Z	E1
001001 000001	Z	E0	E1
001001 000010	E2	E2	E3
001001 000100	FC	FE	FE
001001 000101	Z	FC	FD
001001 001000	F8	FF	FF
001001 001001	Z	F8	F9

FIG. 123

Current code word	Data word		
	Case 1	Case 2	Case 3
001001 001010	FA	FA	FB
001001 010000	F0	F7	F7
001001 010001	Z	F0	F1
001001 010010	F2	F2	F3
001001 010100	F4	F6	F6
001001 010101	Z	F4	F5
001010 000000	C0	Z	C1
001010 000001	Z	C0	C1
001010 000010	C2	C2	C3
001010 000100	DC	DE	DE
001010 000101	Z	DC	DD
001010 001000	D8	DF	DF
001010 001001	Z	D8	D9
001010 001010	DA	DA	DB
001010 010000	D0	D7	D7
001010 010001	Z	D0	D1
001010 010010	D2	D2	D3
001010 010100	D4	D6	D6
001010 010101	Z	D4	D5
001010 100000	C4	Z	C5
001010 100001	Z	C4	C5
001010 100010	C6	C6	C7
001010 100100	CC	CE	CE
001010 100101	Z	CC	CD
001010 101000	C8	CF	CF
001010 101001	Z	C8	C9
001010 101010	Z	Z	CB
010000 000000	34	Z	Z
010000 000001	Z	34	35
010000 000010	1A	1A	1B
010000 000100	1C	1E	1E
010000 000101	Z	1C	1D
010000 001000	18	1F	1F
010000 001001	Z	18	19
010000 001010	1A	1A	1B
010000 010000	10	17	17
010000 010001	Z	10	11
010000 010010	12	12	13

FIG. 124

Current code word	Data word		
	Case 1	Case 2	Case 3
010000 010100	14	16	16
010000 010101	Z	14	15
010000 100000	64	Z	65
010000 100001	Z	64	65
010000 100010	66	66	67
010000 100100	6C	6E	6E
010000 100101	Z	6C	6D
010000 101000	68	6F	6F
010000 101001	Z	68	69
010000 101010	6A	6A	6B
010001 000000	60	Z	75
010001 000001	Z	60	61
010001 000010	62	62	63
010001 000100	7C	7E	7E
010001 000101	Z	7C	7D
010001 001000	78	7F	7F
010001 001001	Z	78	79
010001 001010	7A	7A	7B
010001 010000	70	77	77
010001 010001	Z	70	71
010001 010010	72	72	73
010001 010100	74	76	76
010001 010101	Z	74	Z
010010 000000	40	Z	41
010010 000001	Z	40	41
010010 000010	42	42	43
010010 000100	5C	5E	5E
010010 000101	Z	5C	5D
010010 001000	58	5F	5F
010010 001001	Z	58	59
010010 001010	5A	5A	5B
010010 010000	50	57	57
010010 010001	Z	50	51
010010 010010	52	52	53
010010 010100	54	56	56
010010 010101	Z	54	55
010010 100000	44	Z	45
010010 100001	Z	44	45

FIG. 125

Current code word	Data word		
	Case 1	Case 2	Case 3
010010 100010	46	46	47
010010 100100	4C	4E	4E
010010 100101	Z	4C	4D
010010 101000	48	4F	4F
010010 101001	Z	48	49
010010 101010	4A	4A	4B
010100 000000	08	Z	Z
010100 000001	Z	08	09
010100 000010	0A	0A	0B
010100 000100	0C	0E	0E
010100 000101	Z	0C	0D
010100 001000	08	0F	0F
010100 001001	Z	08	09
010100 001010	0A	0A	0B
010100 010000	00	07	07
010100 010001	Z	00	01
010100 010010	02	02	03
010100 010100	04	06	06
010100 010101	Z	04	05
010100 100000	24	Z	25
010100 100001	Z	24	25
010100 100010	26	26	27
010100 100100	2C	2E	2E
010100 100101	Z	2C	2D
010100 101000	28	2F	2F
010100 101001	Z	28	29
010100 101010	2A	2A	2B
010101 000000	20	Z	21
010101 000001	Z	20	21
010101 000010	22	22	23
010101 000100	3C	3E	3E
010101 000101	Z	3C	3D
010101 001000	38	3F	3F
010101 001001	Z	38	39
010101 001010	3A	3A	3B
010101 010000	30	37	37
010101 010001	Z	30	31
010101 010010	32	32	33

FIG. 126

Current code word	Data word		
	Case 1	Case 2	Case 3
010101 010100	Z	36	36
100000 000001	Z	Z	49
100000 000010	4A	4A	4B
100000 000100	3C	3E	3E
100000 000101	Z	3C	3D
100000 001000	38	3F	3F
100000 001001	Z	38	39
100000 001010	3A	3A	3B
100000 010000	30	37	37
100000 010001	Z	30	31
100000 010010	32	32	33
100000 010100	34	36	36
100000 010101	Z	34	35
100000 100000	24	Z	25
100000 100001	Z	24	25
100000 100010	26	26	27
100000 100100	2C	2E	2E
100000 100101	Z	2C	2D
100000 101000	28	2F	2F
100000 101001	Z	28	29
100000 101010	2A	2A	2B
100001 000000	20	Z	21
100001 000001	Z	20	21
100001 000010	22	22	23
100001 000100	3C	3E	3E
100001 000101	Z	3C	3D
100001 001000	38	3F	3F
100001 001001	Z	38	39
100001 001010	3A	3A	3B
100001 010000	30	37	37
100001 010001	Z	30	31
100001 010010	32	32	33
100001 010100	34	36	36
100001 010101	Z	34	Z
100010 000000	00	Z	01
100010 000001	Z	00	01
100010 000010	02	02	03
100010 000100	1C	1E	1E

FIG. 127

Current code word	Data word		
	Case 1	Case 2	Case 3
100010 000101	Z	1C	1D
100010 001000	18	1F	1F
100010 001001	Z	18	19
100010 001010	1A	1A	1B
100010 010000	10	17	17
100010 010001	Z	10	11
100010 010010	12	12	13
100010 010100	14	16	16
100010 010101	Z	14	15
100010 100000	04	Z	05
100010 100001	Z	04	05
100010 100010	06	06	07
100010 100100	0C	0E	0E
100010 100101	Z	0C	0D
100010 101000	08	0F	0F
100010 101001	Z	08	09
100010 101010	0A	0A	0B
100100 000000	88	Z	B5
100100 000001	Z	88	89
100100 000010	8A	8A	8B
100100 000100	8C	8E	8E
100100 000101	Z	8C	8D
100100 001000	88	8F	8F
100100 001001	Z	88	89
100100 001010	8A	8A	8B
100100 010000	80	87	87
100100 010001	Z	80	81
100100 010010	82	82	83
100100 010100	84	86	86
100100 010101	Z	84	85
100100 100000	A4	Z	A5
100100 100001	Z	A4	A5
100100 100010	A6	A6	A7
100100 100100	AC	AE	AE
100100 100101	Z	AC	AD
100100 101000	A8	AF	AF
100100 101001	Z	A8	A9
100100 101010	AA	AA	AB

FIG. 128

Current code word	Data word		
	Case 1	Case 2	Case 3
100101 000000	A0	Z	A1
100101 000001	Z	A0	A1
100101 000010	A2	A2	A3
100101 000100	BC	BE	BE
100101 000101	Z	BC	BD
100101 001000	B8	BF	BF
100101 001001	Z	B8	B9
100101 001010	BA	BA	BB
100101 010000	B0	B7	B7
100101 010001	Z	B0	B1
100101 010010	B2	B2	B3
100101 010100	B4	B6	B6
100101 010101	Z	B4	B5
101000 000000	98	Z	75
101000 000001	Z	98	99
101000 000010	9A	9A	9B
101000 000100	9C	9E	9E
101000 000101	Z	9C	9D
101000 001000	98	9F	9F
101000 001001	Z	98	99
101000 001010	9A	9A	9B
101000 010000	90	97	97
101000 010001	Z	90	91
101000 010010	92	92	93
101000 010100	94	96	96
101000 010101	Z	94	95
101000 100000	64	Z	65
101000 100001	Z	64	65
101000 100010	66	66	67
101000 100100	6C	6E	6E
101000 100101	Z	6C	6D
101000 101000	68	6F	6F
101000 101001	Z	68	69
101000 101010	6A	6A	6B
101001 000000	60	Z	61
101001 000001	Z	60	61
101001 000010	62	62	63
101001 000100	7C	7E	7E

FIG. 129

Current code word	Data word		
	Case 1	Case 2	Case 3
101001 000101	Z	7C	7D
101001 001000	78	7F	7F
101001 001001	Z	78	79
101001 001010	7A	7A	7B
101001 010000	70	77	77
101001 010001	Z	70	71
101001 010010	72	72	73
101001 010100	74	76	76
101001 010101	Z	74	75
101010 000000	40	Z	41
101010 000001	Z	40	41
101010 000010	42	42	43
101010 000100	5C	5E	5E
101010 000101	Z	5C	5D
101010 001000	58	5F	5F
101010 001001	Z	58	59
101010 001010	5A	5A	5B
101010 010000	50	57	57
101010 010001	Z	50	51
101010 010010	52	52	53
101010 010100	54	56	56
101010 010101	Z	54	55
101010 100000	44	Z	45
101010 100001	Z	44	45
101010 100010	46	46	47
101010 100100	4C	4E	4E
101010 100101	Z	4C	4D

FIG. 130

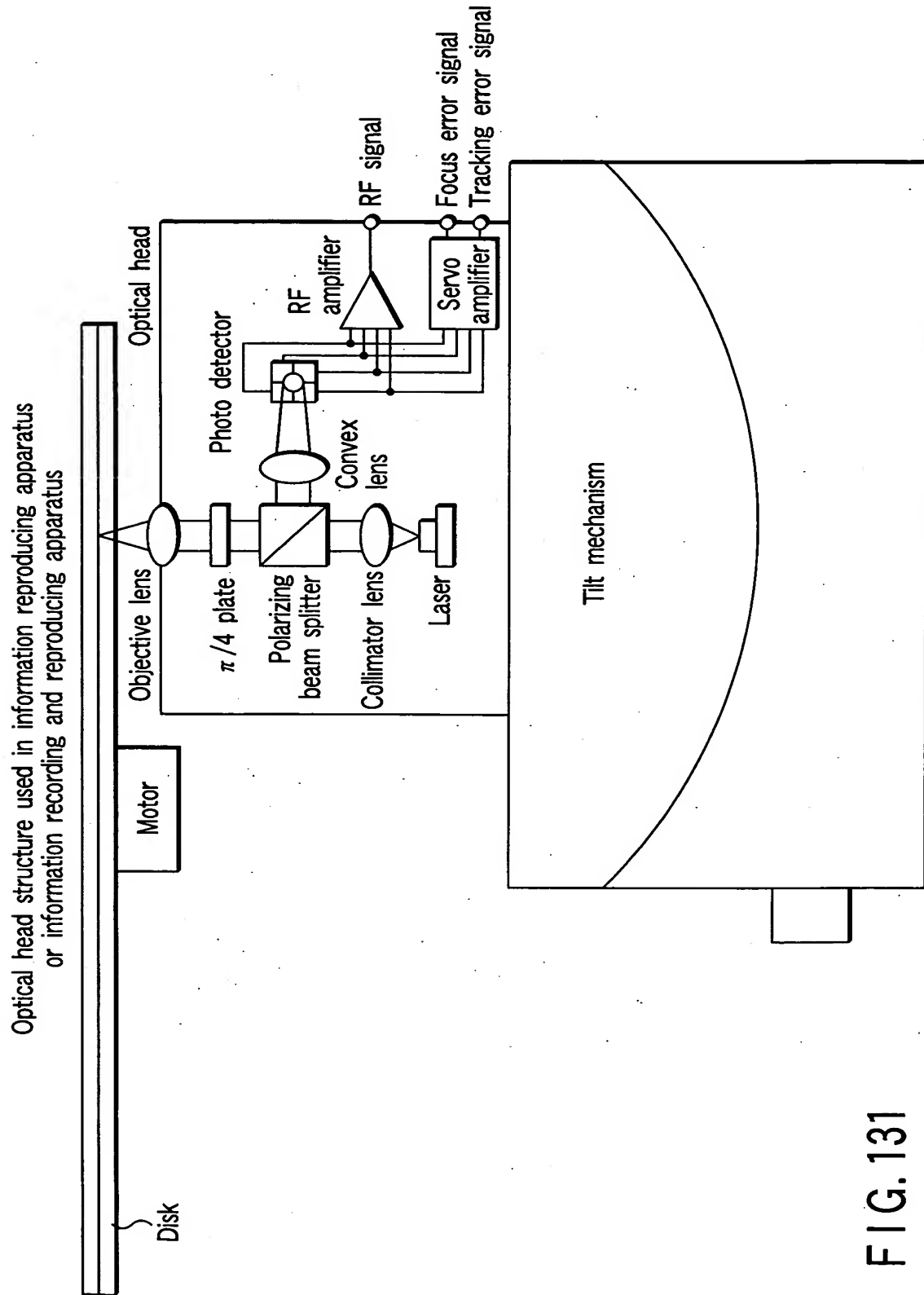
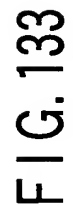


FIG. 131



FIG. 132



Method for identifying sync frame position in sector from
arrangement of 3 continuous sync codes

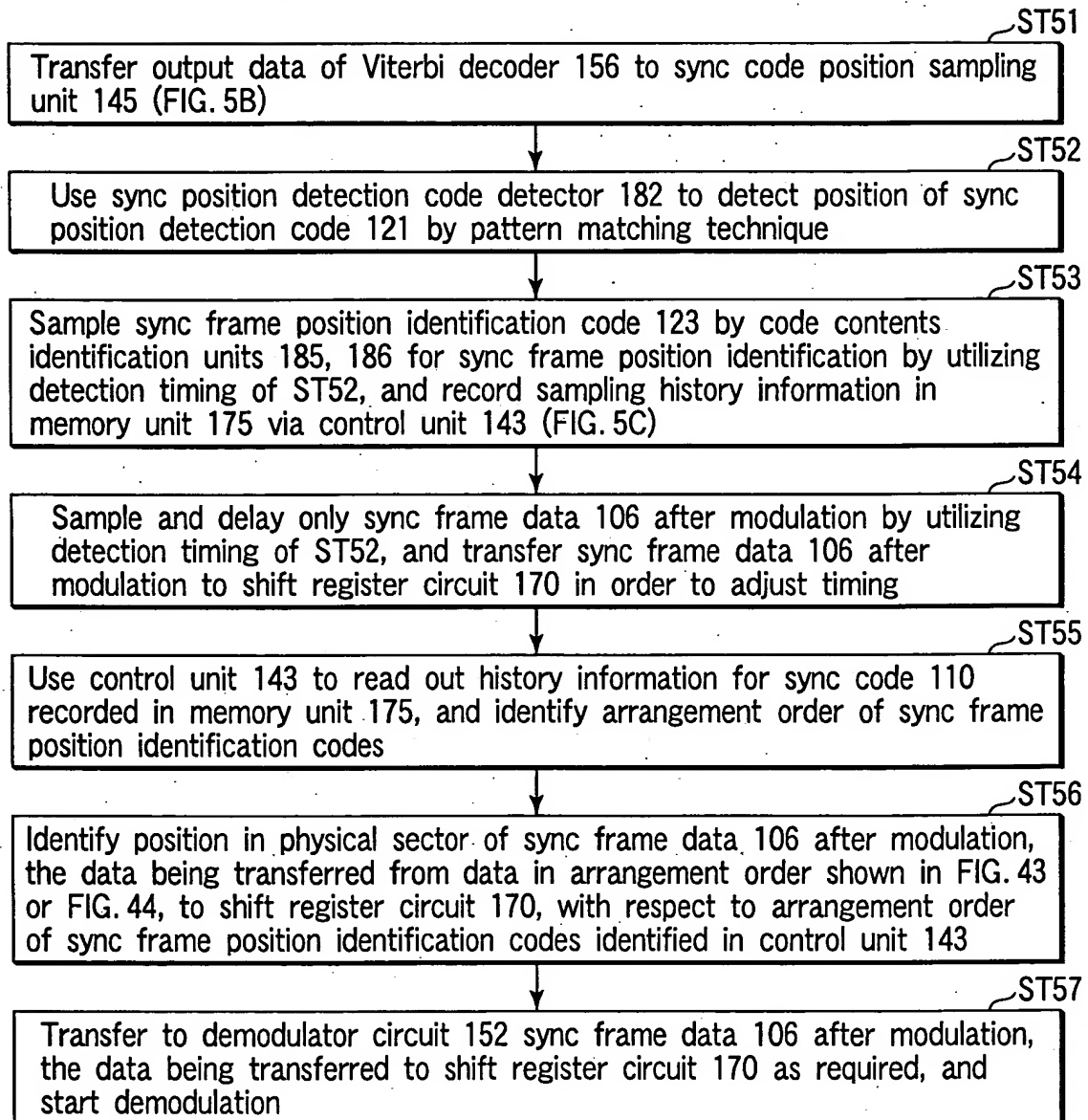


FIG. 134

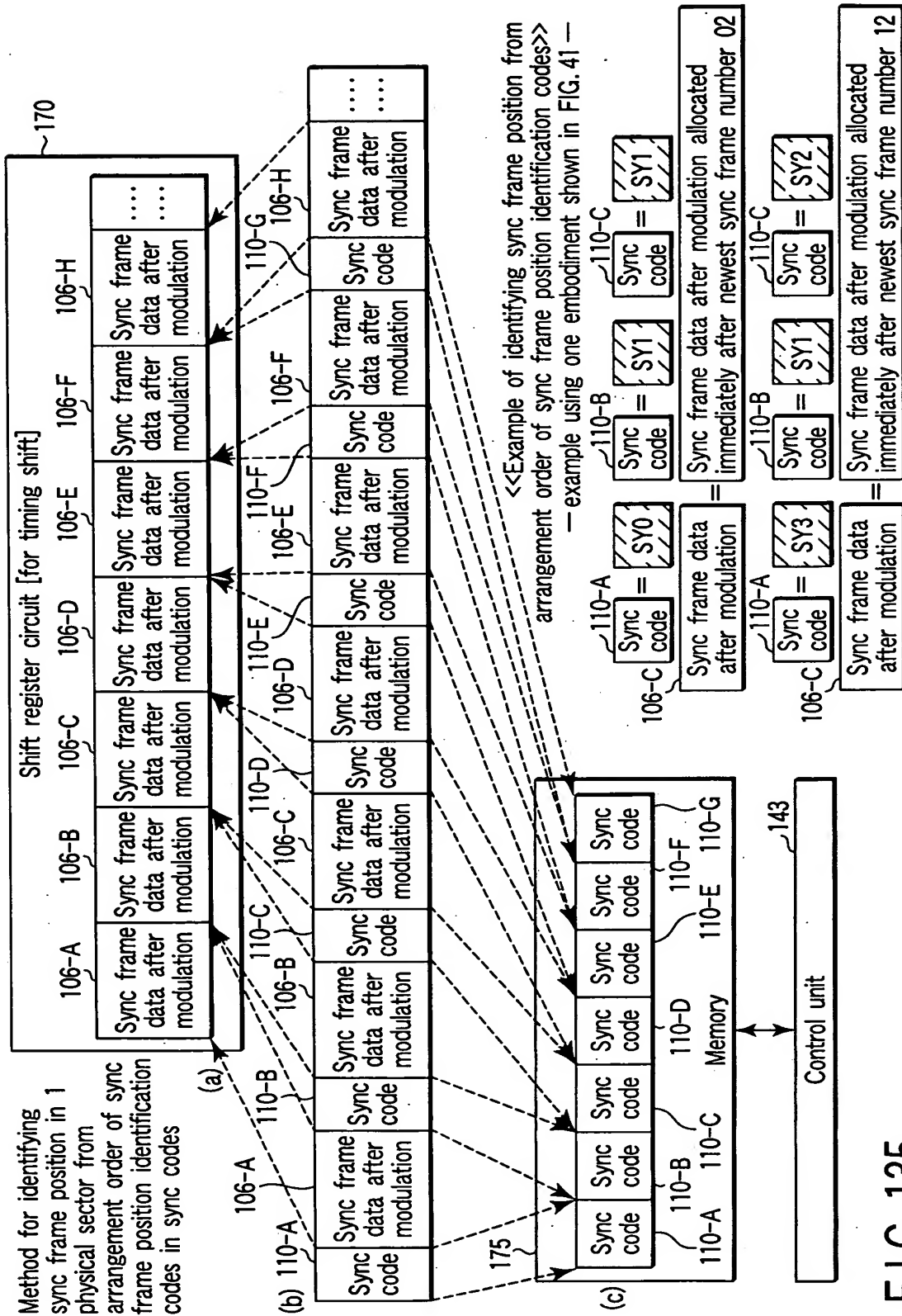


FIG. 135

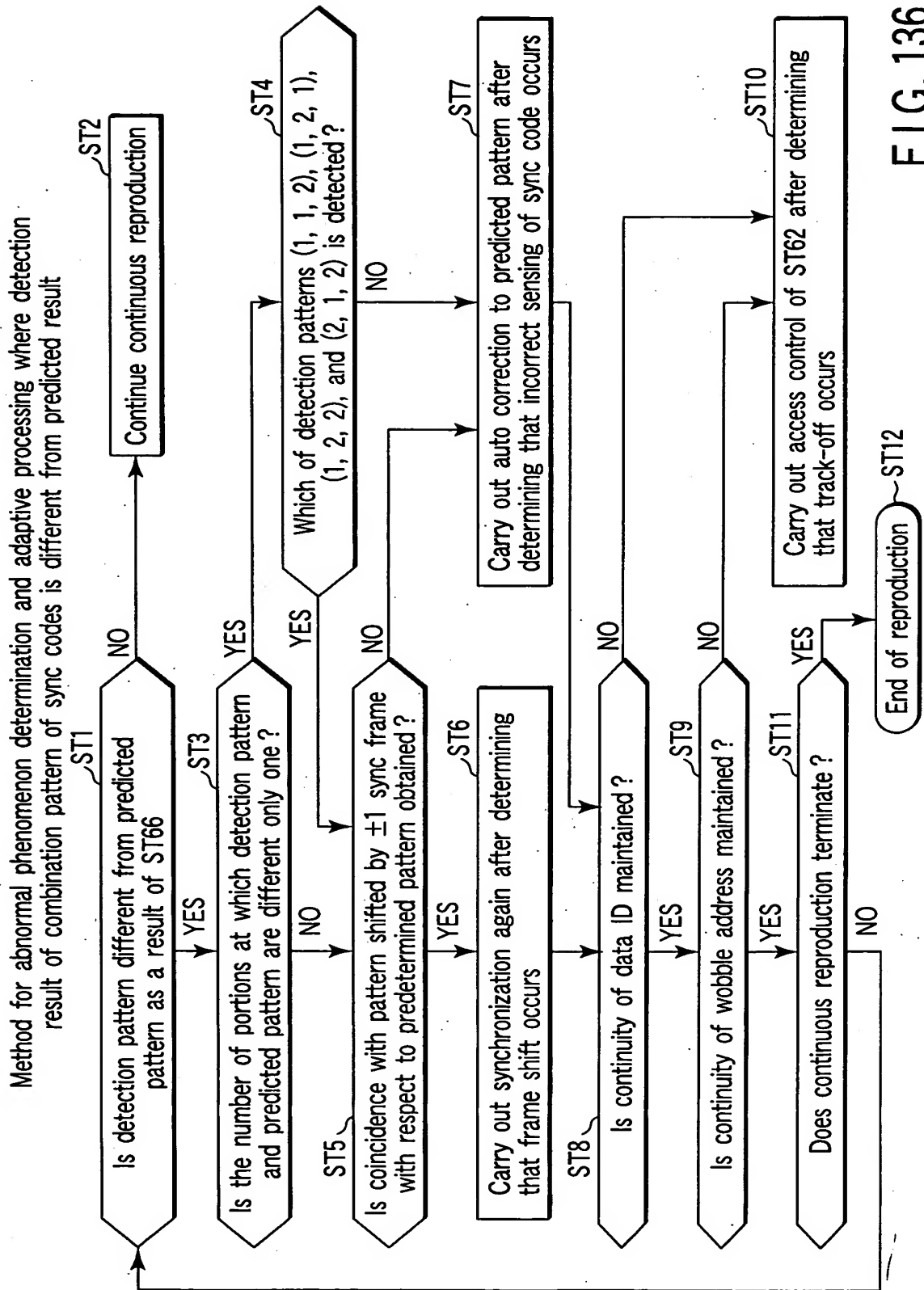


FIG. 136

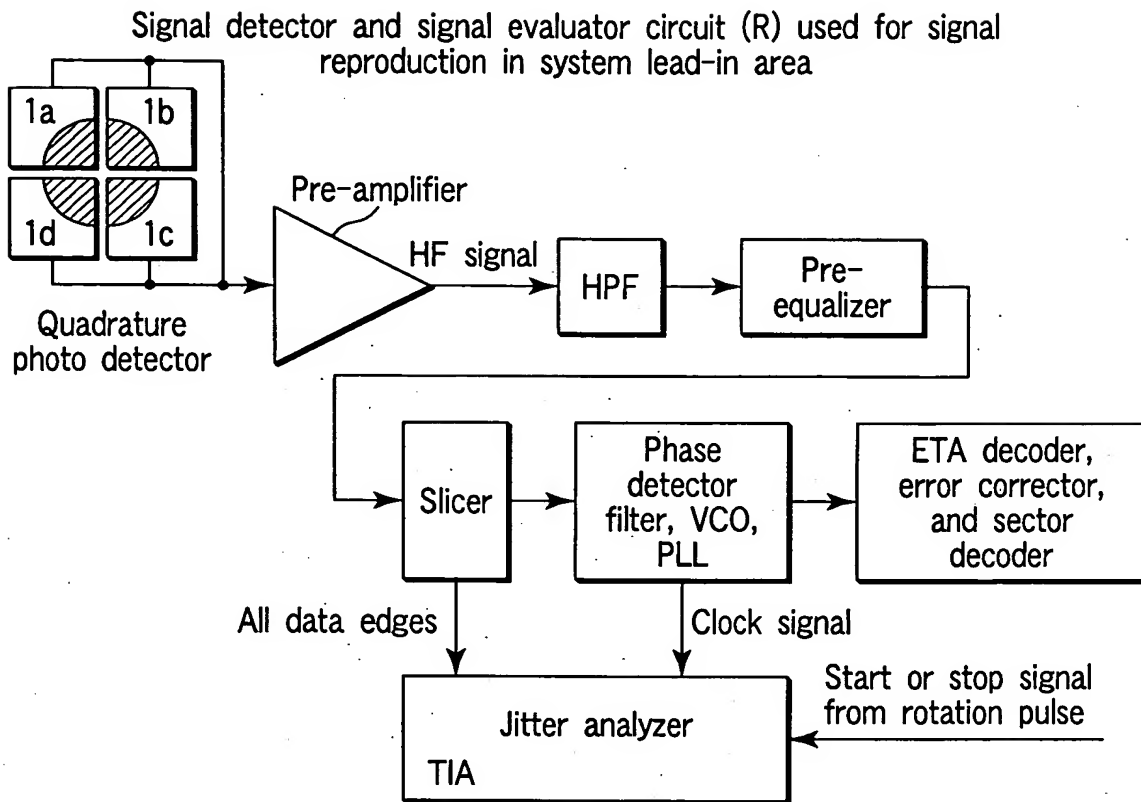


FIG. 137

Slicer circuit used for signal reproduction in system lead-in region

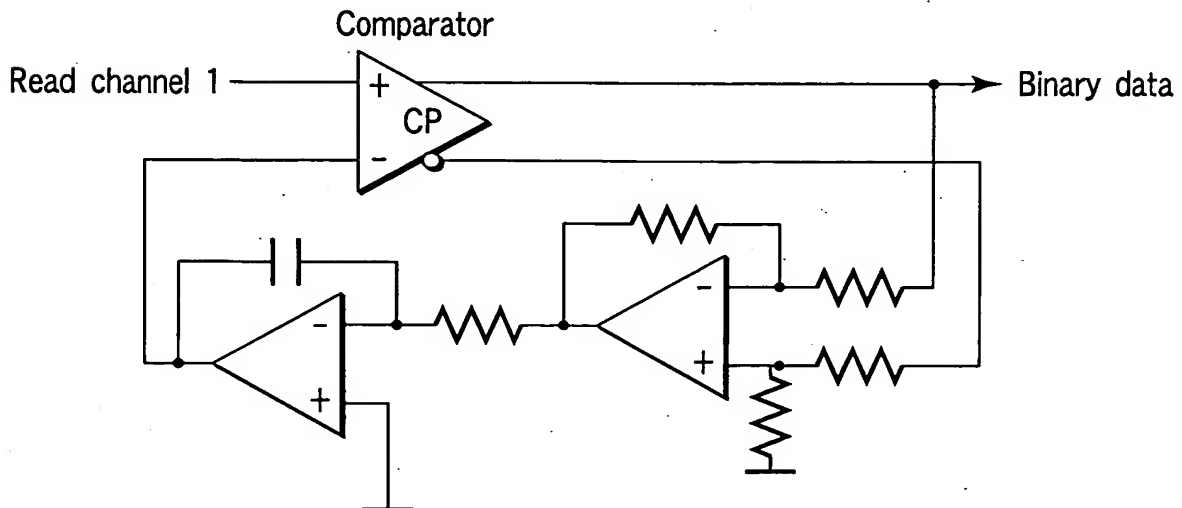


FIG. 138

Detector circuit (S) used for signal detection in data lead-in region, data region, and data lead-out region

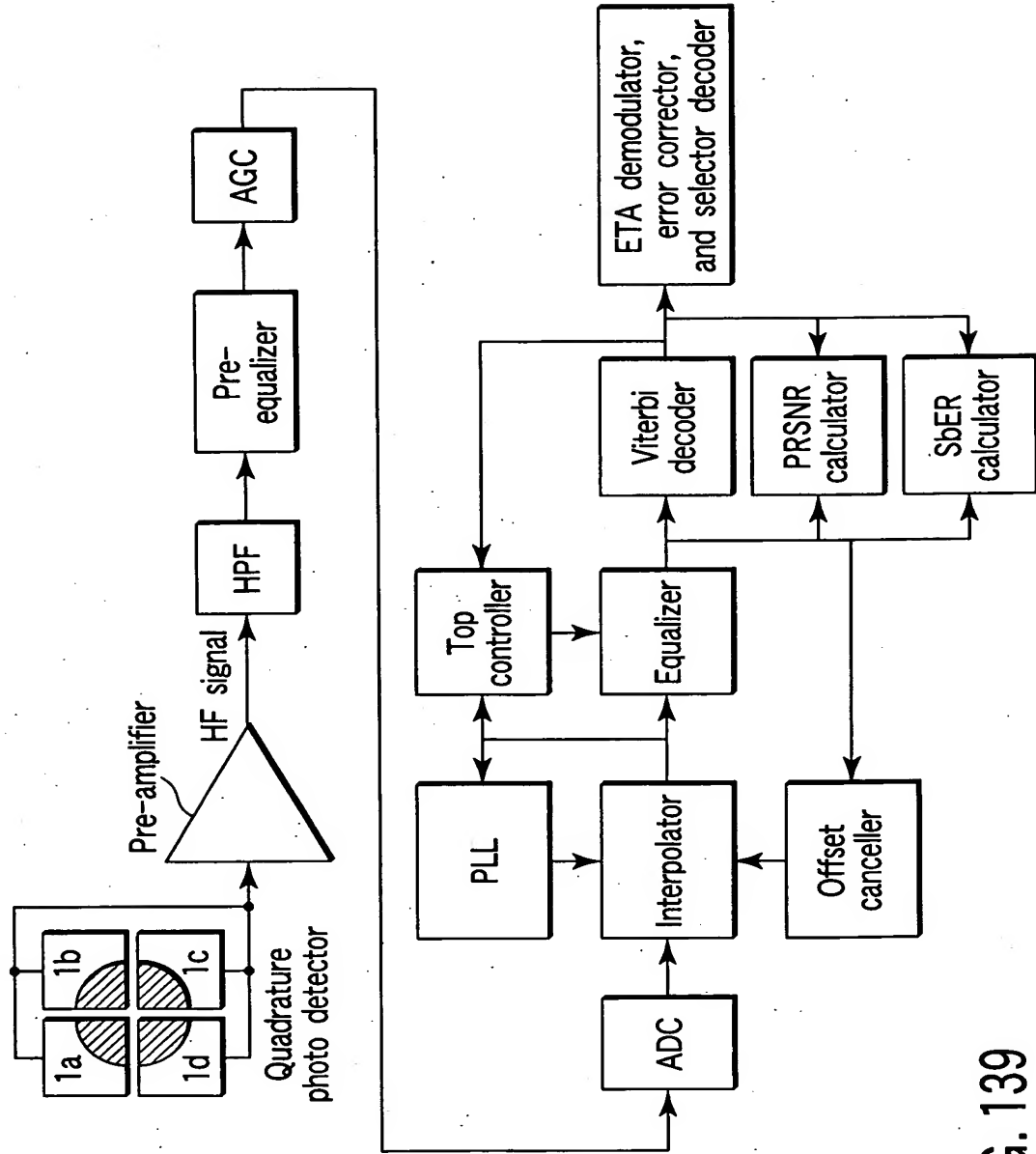


FIG. 139

Viterbi decoder

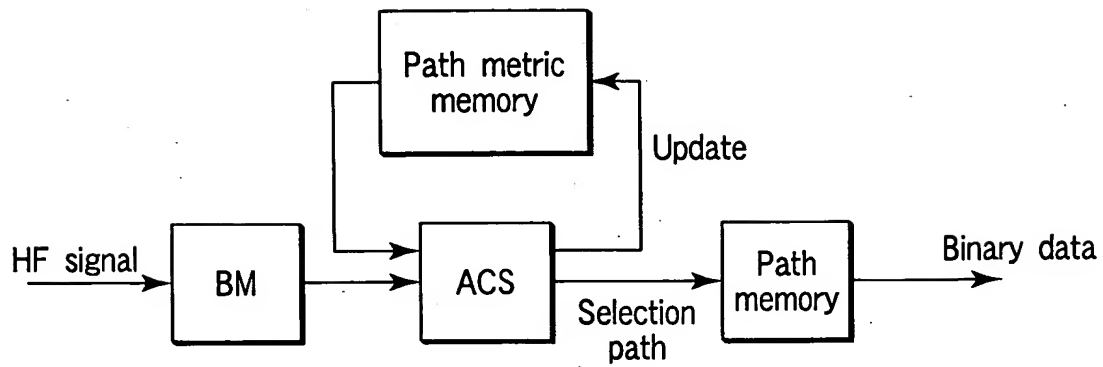


FIG. 140

State transition of PR(1,2,2,2,1) channel combined with ETM code

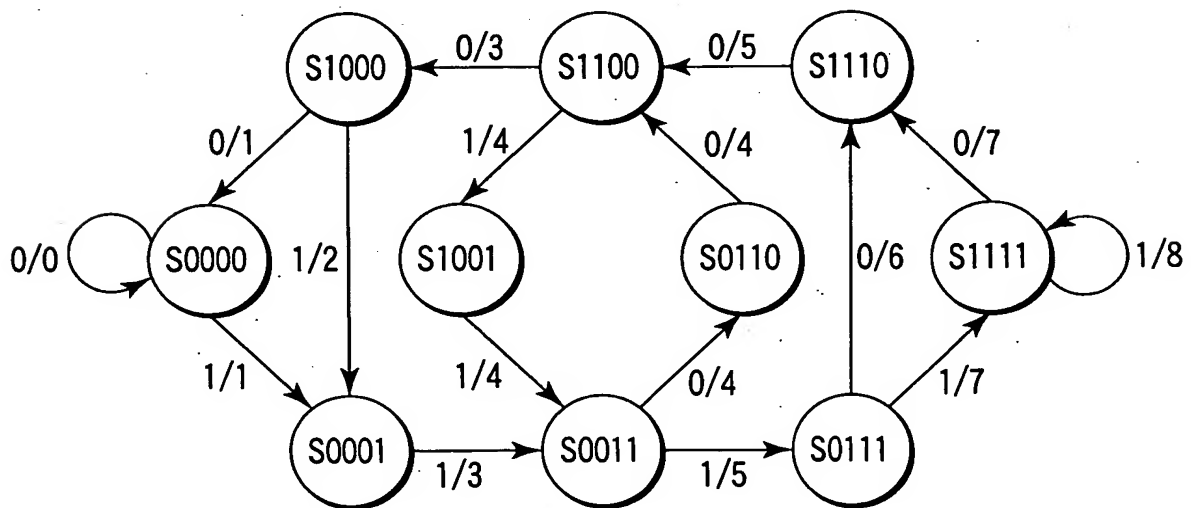


FIG. 141

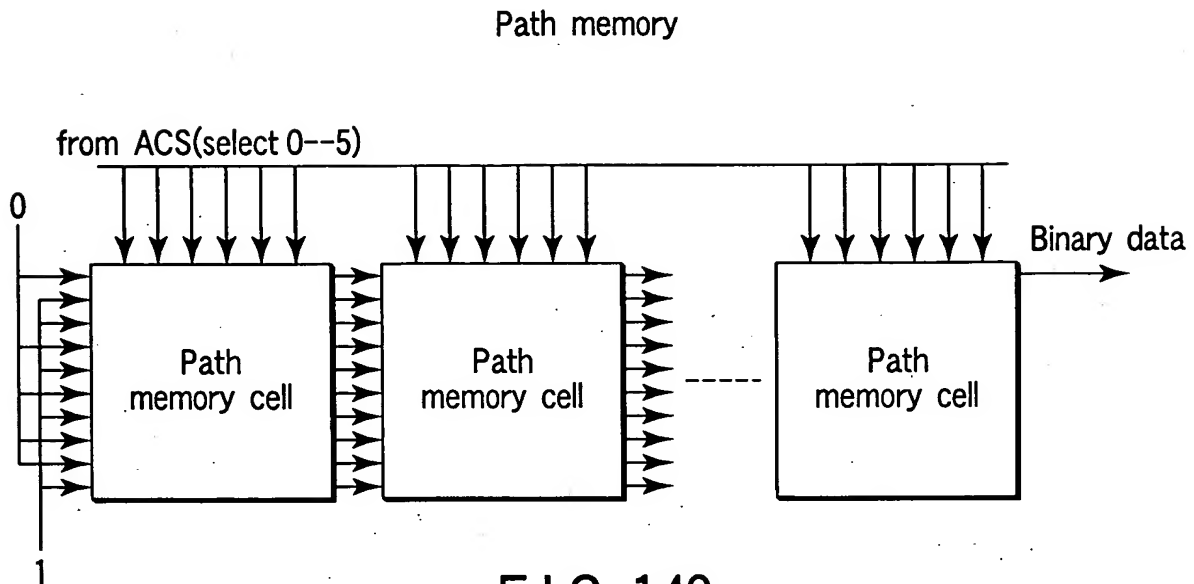


FIG. 142

I/O of path memory cell

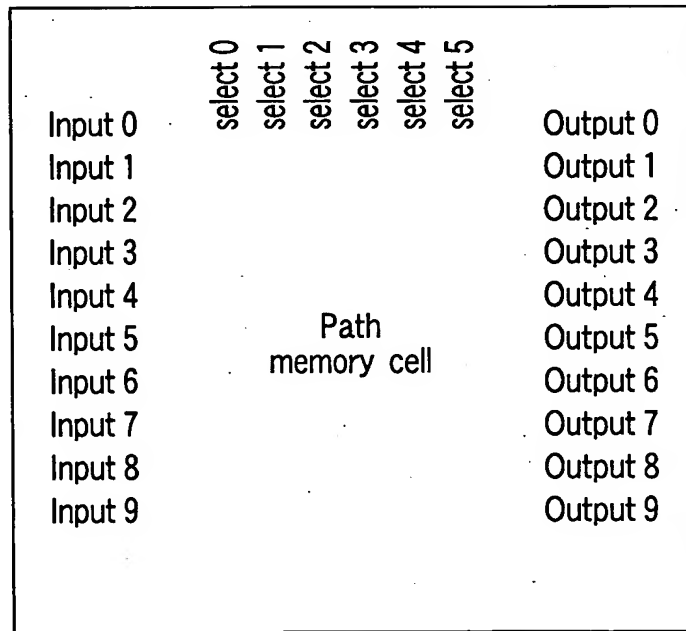


FIG. 143

Configuration of path memory cell

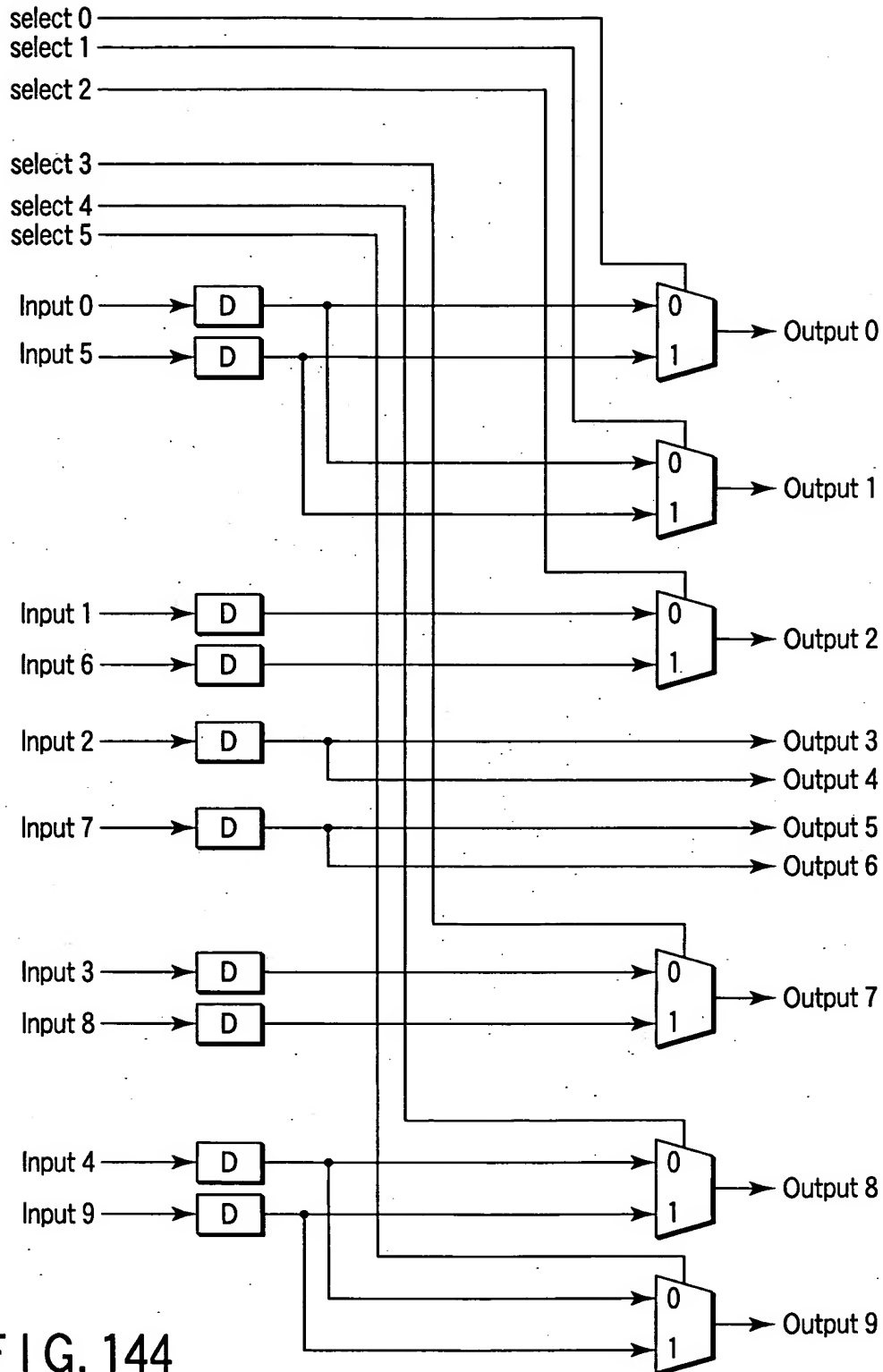


FIG. 144